(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 March 2011 (17.03.2011)

PCT

(10) International Publication Number
WO 2011/031175 A1

(51) International Patent Classification:
*G06F 1/20* (2006.01) *G06F 1/32* (2006.01)

(21) International Application Number:
PCT/PL2010/050050

(22) International Filing Date:
14 September 2010 (14.09.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
P 389 037 14 September 2009 (14.09.2009) PL
P 390 201 18 January 2010 (18.01.2010) PL

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published**:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) Title: METHOD OF POWER CONTROL IN MICROPROCESSOR STRUCTURES AND A POWER CONTROL SYSTEM IN MICROPROCESSOR STRUCTURES

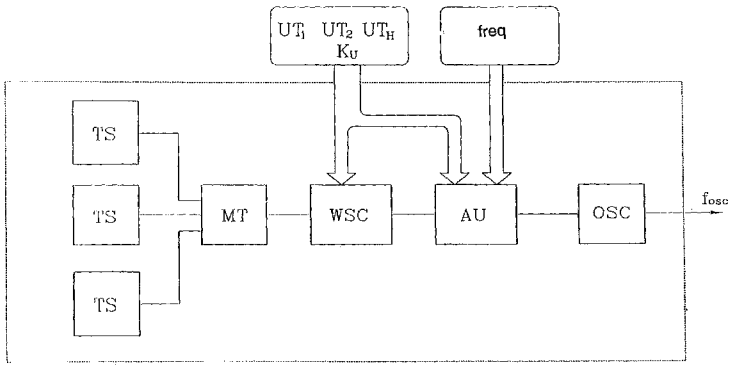


Fig.6

(57) Abstract: A power control system in microprocessor structures has an arbitration unit (AU), connected via a characteristic shaping unit (WSC) and a maximum temperature (MT) selection system to at least one temperature sensor (TS), in addition the arbitration unit (AU) is connected to the retuned oscillator (OSC).

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# Method of power control in microprocessor structures and a power control system in microprocessor structures

The invention concerns a method of power control in microprocessor structures and a power control system in microprocessor structures.

The microprocessor capacity, defined as the number of processor logical operations executed in a time unit, is proportional to the number of transistors contained in the processor structure and the clock oscillator frequency. On the other hand both mentioned parameters have also a direct and proportional impact on the amount of thermal power dissipated in the microprocessor structure. As modern processes enable microprocessors adapted to operate with very high frequencies to be made, the maximum processor capacity is limited mainly by thermal effects arising from a high concentration of heat sources in a small volume of a processor structure. To effectively protect a microprocessor structure against overheating, at the same time utilising its full available capacity, specific circuits for control and monitoring of both the value of thermal power dissipated and the processor capacity must be applied.

Typical methods for reducing the heat dissipated in the processor structure use a dynamic control of one of the parameters decisive to the value of the thermal power dissipated, such as reducing the oscillator frequency or decreasing the microprocessor supply voltage. However, direct control methods do not allow the available processor capacity to be fully utilised; also step retuning of oscillator frequency is disadvantageous to the system, because the likelihood of hazard occurrence is increased. Therefore new processor capacity management strategies are sought, which would allow processor calculation capabilities to be better utilised.

A process and apparatus for minimising energy consumption by battery powered microprocessor devices are known from patent descriptions US 6 883 104 and US 7 340 625. The description unveils a process and apparatus for reducing the power consumption of microprocessor-based devices by reducing the frequency of the oscillator governing the logical operations of the processor during periods of use in

which high system performance is not critical. In one embodiment of apparatus the microprocessor is controlled by an additional monitor circuit containing a programmable frequency oscillator. In another embodiment a hardware monitor circuit tracks microprocessor instructions to determine periods of use when high processor performance is not critical. The shift in oscillator frequency is performed by flip-flop latch circuits, which select frequencies to control the microprocessor.

A synchronic system containing a logic controller (e.g. a microprocessor) is known from description US 7 543 163. It may be set on stand-by with a low power consumption by switching the oscillator off. A quick start oscillator remains in the off state to preserve energy but it responds quickly and supplies clock signals to the logic controller so that it can respond to new circumstances. For instance, a supply voltage drop may be among such circumstances. Then a low voltage detector activates the quick start oscillator, which in turn takes the controller circuit out of the "sleep" state. The controller runs a procedure for identifying the cause of taking out of the "sleep" state, and next it responds to the ensuing circumstances, and switches the quick start oscillator off. The description shows a quick start oscillator, a low voltage detector circuit and the structure of the new DAC contained in the low voltage detector circuit.

A method and a system for optimal thermal control of processor structures is known from description US 7 464 278, in which the temperature control in the processor structure is combined with predicting. The additional supervisory program analyses the previously recorded course of past events and the list of instructions foreseen to be executed by the processor in the immediate future, next based upon the analysis results it calculates the system operating parameter that controls the system temperature. If the predicted thermal parameter values are estimated higher than the allowable values, the operating parameter will be reduced so that the predicted thermal parameter value is lower than the allowable value. The operating parameter determines the value of supply voltage or oscillator frequency. The system presented in the description contains at least one meter for checking if the thermal limitation has not been exceeded, at least one calculator for determining the future time interval in which the temperature will be maintained within the set limits, at least one controller for setting up the oscillator frequency and the processor supply

voltage, where the controller calculates the time interval in which the parameter limit value will be exceeded and next it reduces at least one of the parameters such as frequency or voltage to bring the power consumption down to a level at which the parameter limit value is not exceeded.

A method of microprocessor performance control is known from description US 7 353 414, the method adapts to variable requirements concerning the processor performance, at the same time providing the predetermined programmed performance. The method according to that invention tolerates changes in momentary processor activity in relation to the predetermined programmed processor performance, including exceeding of the programmed value as well, however the average value of the programmed processor performance is maintained at a constant level.

Apart from the necessary components such as a temperature sensor and retuned oscillator the mentioned control methods require fast storage blocks to be used, in which past events are recorded as well as a list of instructions waiting for execution and specific supervisory programs.

In the solution according to the invention the control may be substantially simplified, without the need to use analysing circuits.

According to the invention the method of power control in microprocessor structures consisting in the clock frequency control and supply voltage control based on the measured temperature values for each of the processor cores is characterised by the fact that prior to the actual control process the parameter values decisive to the control process are set up, such as: the allowable temperature limit value in the microprocessor structure, the first limit temperature value, the second limit temperature value, the hypothetical limit temperature value and the value of the parameter determining the degree of oscillator response to the microprocessor temperature change between the second limit temperature value and the hypothetical limit temperature value, next during the current check, the value of the parameter determining the required processor capacity is entered systematically into the control circuit, and then on the basis of the measured temperature values

and the set parameter values via the arbitration unit the control method is determined so that until none of the temperature sensors records the exceeding of the second limit temperature value, the oscillator output frequency is determined in accordance with the value of the parameter determining the required microprocessor capacity, whereas if at least one of the temperature sensors records the exceeding of the second limit temperature the oscillator frequency value is decreased until the highest temperature value measured by any sensor is lower than the value of the first limit temperature, and then the set oscillator frequency value is determined in accordance with the value of the parameter determining the required microprocessor capacity.

Dynamic control parameters are determined with set up parameters such as: the hypothetical limit temperature value and the parameter determining the degree of oscillator response to the microprocessor temperature change, the value of which is determined by the analogue signal gain coefficient in the signal circuit between the temperature sensor and the oscillator.
The subsequent set up values of the required oscillator frequency may be selected by a computer program with the successive approximation method.
Selected parameters of the microprocessor structure are measured, such as: the microprocessor structure temperature, supply voltage, temperature increase rate, power consumption for a specific past time interval, next the optimal oscillator output frequency value is predicted for a specific future time interval, then the division value for the frequency divider is set up, which is the ratio of the predicted optimal output frequency of the retuned oscillator to the standard oscillator frequency, next the output frequency of the retuned oscillator is checked.

The power control system in microprocessor structures containing at least one temperature sensor and a circuit of voltage-controlled oscillator is characterised by an arbitration unit, connected via the characteristic shaping unit and the maximum temperature selection system to at least one temperature sensor, in addition the arbitration unit is connected to the retuned oscillator.

The power control system has an arbitration unit, connected to the characteristic shaping unit and the retuned oscillator, in addition the arbitration block is fitted with input circuits for the signal determining the set frequency.

The power control system may have a prediction unit, which is connected to the temperature measurement unit, the supply current measurement unit, the past energy consumption measurement unit, the future predicted energy consumption estimation unit, in addition the prediction unit is connected to the frequency divider, which in turn is connected to the retuned oscillator and the comparing unit, and this one is connected to the standard oscillator and through the forming unit to the retuned oscillator.
The comparing unit contains a phase detector circuit. The comparing unit contains phase detector and frequency detector circuits.
The forming unit has a low-pass filter. The forming block has a charge pump.

The invention is explained in drawings.
Fig. 1, fig. 2, fig. 3 present diagrams of processor structure temperature during execution of the same set sequence of instructions for various applied methods of power control – fig. 1 - without power control; fig. 2 - with classic dynamic power control; fig. 3 - with dynamic power control using one of invention embodiments – with the predictor.
Fig. 4 explains the temperature control method according to the invention, fig. 5 explains the temperature control method with the use of optimal selection of the required oscillator frequency value, fig. 6 presents the block diagram of the power control system for microprocessor structures in the first embodiment. Fig. 7 presents the block diagram of the power control system for microprocessor structures in the second embodiment, fig. 8 presents the block diagram of the power control system for microprocessor structures in the embodiment with the predictor, fig. 9 presents an embodiment example of the power control system for microprocessor structures in the first variant, fig. 10 presents an embodiment example of the power control system for microprocessor structures in the first variant with an option of automatic selection of the optimal required oscillator frequency, fig. 11 presents an embodiment example of the power control system for microprocessor structures in the second variant.

Fig. 1 illustrates the system operation without any control, whatever the technique. The presented course of power consumption corresponds to the set work that a system operating at its full efficiency would perform in 200 time units. A system operating in this mode would be damaged because the structure temperature would exceed the maximum allowable value $T_{MAX}$ between the 170-th and 180-th time unit. Fig. 2 presents changes in the temperature of a system controlled by a classic dynamic voltage control technique combined with the dynamic frequency control. All basic dynamic power management techniques require the knowledge of threshold temperatures, designated in the graph as $T\_{HI}$, $T\_{LO}$, which define when a change in the system operation state (maximum and reduced performance) should be made. The supply voltage and system operation frequency dynamic reduction methods are applied here to provide as high processor capacity as possible without the risk of system overheating. The oscillator state value graph, which is multiplied by 10 to obtain more legible characteristics and designated as $CLK\_{dvs}$, is also presented in this drawing. The value “1” (seen in the graph as 10%) means the full system performance, while the value “2” (seen as 20%) – operation with a reduced power consumption. The system performs the set work within 219.8 time units reducing its efficiency twofold. Fig. 3 presents temperature changes in a dynamically controlled system by applying prediction according to the invention. In this case the method increases the efficiency by c.a. 5.3%. An increase in efficiency is usually related to an increase in the temperature of the microprocessor structures, but it should be emphasised that the proposed method exercises control over the operating temperature and ensures that its maximum allowable value is not exceeded.

The power control method in microprocessor structures is explained by the graph shown in fig. 4. If the microprocessor operates at its full capacity its structure temperature oscillates between the two set limit temperatures $T_1$ and $T_2$. After the temperature $T_2$ is exceeded, the oscillator frequency is controlled by a temperature sensor signal. Such control causes temperature decrease in accordance with the curve approaching the $T_H$ temperature value. After the limit temperature $T_1$ is reached, the system is reconfigured so that its frequency is controlled by the set microprocessor capacity. It is advantageous to decrease the temperature oscillation frequency as it extends the relative time of microprocessor operation with the

required frequency, in addition the frequency of flip-flops between the operation mode with the required frequency value and the operation mode where the OSC oscillator frequency is controlled by the temperature measuring system declines. Therefore it is appropriate to use a procedure that allows the required frequency optimal value to be selected. The required frequency optimal value may be estimated on the basis of measurement of the period of temperature oscillation between the $T_2$ and $T_1$ value. Another method for ensuring a faster matching is the successive approximation method, which is explained by the graph presented in fig. 5. The method for selection of the optimal oscillator OSC frequency consists in that every time the limit temperature $T_2$ is exceeded, the required frequency value is decreased, in other words, exceeding the limit temperature $T_2$ results in implementing a new adjusted required frequency value. In the initial period the new required value has no influence on the oscillator OSC frequency because in this period ($\Delta t1$) the oscillator OSC frequency is determined by the circuit analysing the microprocessor structure temperature, however after a lapse of the time ($\Delta t1$) the oscillator OSC frequency is determined by the new adjusted value of required frequency. By analysing the course of changes in the microprocessor structure temperature after making an adjustment of the required frequency value and a lapse of time ($\Delta t1+\Delta$), from the moment the limit value $T_2$ has been exceeded and the new required frequency value has been set, the arbitration system AU makes verification of the adjustment. The new adjusted value of the required frequency will be accepted if after a lapse of time ($\Delta t1+\Delta$) the microprocessor structure temperature is higher than T1, whereas if after a lapse of time ($\Delta t1+\Delta$) the microprocessor structure temperature is lower than T1, the implemented adjustment will be cancelled and the previous value of the required frequency will be restored. The two mentioned cases are presented in fig. 5, where: “W-R” – adjustment rejection, “W-A" – adjustment acceptance.

The process of optimal parameter selection is multistage, and the adjustment value may be a variable parameter. The optimal adjustment value may be selected with one of successive approximation methods used in A/D conversion systems: either the method of small equal steps or the method of successive approximation where adjustment values implemented and verified successively remain in a ratio 8:4:2:1

against one another. For example: the first adjustment changes the set frequency value by 50% against the maximum value (point A), the second adjustment changes the previous already verified value by 25% point (B), the third one by 12.5%, etc.

$UT_1$, $UT_2$ and $UT_H$ are values, for instance of voltage in the system embodiment corresponding to the temperatures - the first limit one, the second limit one and the hypothetical one. $K_u$ is a parameter determining the degree of oscillator response to a temperature change.

The predictive method of dynamic control constituting an invention variant may be applied for temperature control, uses the fact identified as a result of research that having reached the upper threshold $T_{HI}$ the processor temperature does not always approach the maximum allowable value $T_{MAX}$. In this case the processor may continue its operation at the same level of intensity. The temperature diagram presented in fig. 3 illustrates this case. The application of the predictive method for oscillator frequency control in this case enables the execution time of a set instruction series to be shortened by more than 5%.

The power control system in microprocessor structures presented in fig. 6 has at least two temperature sensors TS. The temperature sensors TS are connected to the maximum temperature selection system MT, which transmits the selected signal to the characteristic shaping unit WSC, which subject to values of selected input parameters of the control process performs shaping of the transitional characteristics for a selected analogue signal of the temperature sensor TS. The characteristics shaping unit WSC is connected to the arbitration system AU, to which also selected input parameters of the control process are entered, such as: the first limit temperature value $T_1$ and the second limit temperature value $T_2$ and the parameter determining the value of the oscillator OSC required frequency. Depending on the result of comparison of the maximum measured temperature to the required control process input parameters, the oscillator OSC frequency is determined directly on the basis of the value of the required oscillator OSC frequency, provided that the second limit temperature value $T_2$ has not been exceeded by any of the sensors TS. When at least one of the temperature sensors TS records exceeding of the second limit temperature $T_2$ the oscillator OSC

frequency is determined in relation to the measured temperature (periods $\Delta t1$, $\Delta t2$ in fig. 1). The temperature measurement circuit gradually decreases the oscillator OSC frequency value until the highest temperature value measured by any of the temperature sensors TS is lower than the first limit temperature value $T_1$, and then it re-determines the required oscillator OSC frequency value in accordance with the value of the parameter determining the required microprocessor capacity. The dynamic parameters of the power control process are determined by setting the hypothetical temperature limit value $T_H$ and the values of signal gain coefficient in the characteristic shaping unit WSC. Both mentioned parameters determine the microprocessor structure cooling rate between the set second limit temperature value $T_2$ and the set first limit temperature value $T_1$. The hypothetical temperature limit value $T_H$ is an auxiliary parameter determining the control process dynamics. It is the temperature value that the microprocessor structure would reach in the case of heavy loading of the processor and with application of the oscillator OSC frequency control only on the basis of its temperature measurement.

The system of power control in microprocessor structures presented in fig. 7 in the second embodiment has an arbitration unit AU, connected to the characteristic shaping unit constituting in this case also a temperature sensor, and the retuned oscillator OSC, in addition the arbitration unit is fitted with input circuits for the signal determining the required frequency.

In the invention embodiment presented in fig. 8 the prediction unit PR on the basis of signals supplied by the temperature sensor unit TS, the supply current measurement unit IDD, the past energy consumption measurement unit ESR and the future energy consumption estimation unit OS determine the frequency divider FD value. The frequency divider FD calculates the quotient of the output frequency of the retuned oscillator OSC and the standard oscillator $F_0$ frequency, and the result of this operations is compared in the comparing unit PD/PFD. The output signal of the comparing unit PD/PFD controls the forming unit CP/LPF, which may constitute a low-pass filter or a charge pump circuit. Subject to the comparison result the output signal in the forming unit CP/LPF will gradually increase or decrease, and as this signal controls the frequency of the retuned oscillator OSC, the output frequency of the retuned oscillator OSC will be stabilised. The stabilised

value of frequency of the retuned oscillator OSC will be the product of the standard oscillator $F_0$ frequency and the division value entered into the frequency divider FD.

This method of control of output frequency of the retuned oscillator OSC ensures a smooth transition to the new set frequency, being a product of the standard oscillator $F_0$ frequency and the division value of frequency divider FD. Thus the hazard is much less likely to occur than in devices with a step oscillator frequency change e.g. resulting from disturbances in the switching process.

This method of control of output frequency of the retuned oscillator OSC ensures a smooth transition to the new set frequency, being a product of the standard oscillator $F_0$ frequency and the division value of frequency divider FD. Thus the hazard is much less likely to occur than in devices with a step oscillator frequency change e.g. resulting from disturbances in the switching process.

Fig. 9 presents an embodiment example of the power control system in the first variant. The system contains one monolithic temperature sensor TS based on two P-N connectors biased with various currents, with a constant relative ratio of values. A structure like this fitted with additional semiconductor components shows a proportional dependence of the current on the temperature. The temperature sensor TS is connected directly to the WSC unit based on three operating amplifiers. Dynamic control process parameters have been determined by a selection of the gain coefficient in the signal circuit and the values of biasing voltages. The output signal from the WSC unit is supplied by an analogue switch with the oscillator OSC, with the oscillation frequency controlled with varicaps. The OSC oscillator is also connected via an analogue switch to the digital to analogue converter DAC, through which the value of the required oscillator OSC frequency is determined.

Fig. 10 presents an embodiment example of the power control system in the first variant. An extended arbitration system AU, adapted to work with the approximating register SAR is used in the system. In this application the arbitration system AU is additionally fitted with two sampling comparators SC and delaying components DEL1, DEL2. The application enables the full available processor capacity to be used without the fear of exceeding the allowable processor operating conditions.

Thanks to the application of successive approximation, which enables the optimal set oscillator frequency to be gradually selected, the amplitude and frequency of temperature oscillations are minimised, as well as the operating mode changing frequency. Thus the processor operation periods with the required optimal oscillator frequency determined by a program are extended.

Fig. 11 presents an embodiment example of the power control system in the second variant. In this system the temperature sensor function is performed by bipolar semiconductor components located in the transition characteristic shaping unit WSC.

In the presented application examples the oscillator frequency is under control. It is obvious that the presented power control methods may be executed also by the microprocessor structure supply voltage control or which is particularly advantageous, by a simultaneous change maintaining appropriate proportions of both parameters.

**Patent claims**

1. Power control method in microprocessor structures consisting in the clock frequency control and supply voltage control on the basis of measured temperature values for each of the processor cores, **characterised in that**
   - before the actual control process the values of parameters decisive to the control process are set, such as: the allowable temperature limit value in the microprocessor structure, the first limit temperature value, the second limit temperature value, the hypothetical limit temperature value and the value of the parameter determining the degree of oscillator response to the microprocessor temperature change between the second limit temperature value and the hypothetical limit temperature value,
   - next during the current check, the value of the parameter determining the required processor capacity is entered systematically into the control circuit,
   - then on the basis of the measured temperature values and the set parameter values via the arbitration unit the control method is determined so that until none of the temperature sensors records the exceeding of the second limit temperature value, the oscillator output frequency is determined in accordance with the value of the parameter determining the required microprocessor capacity,
   - however if at least one of the temperature sensors records the exceeding of the second limit temperature the oscillator frequency value is decreased until the highest temperature value measured by any of the sensors is lower than the value of the first limit temperature,
   - and then the set oscillator frequency value is determined in accordance with the value of the parameter determining the required microprocessor capacity.
2. The method as claimed in claim 1, **characterised in that** the dynamic control parameters are determined with setting parameters such as: the hypothetical limit temperature value and the parameter determining the degree of oscillator response to the microprocessor temperature change, the value of

which is determined by the analogue signal gain coefficient in the signal circuit between the temperature sensor and the oscillator.

3. The method as claimed in claim 2 **characterised in that** the subsequent setting values of the required oscillator frequency are selected by a computer program by application of the successive approximation method.
4. The method as claimed in claim 1 **characterised in that**
   - during temperature controlling selected parameters of the microprocessor structure are measured, such as: the microprocessor structure temperature, supply voltage, temperature increase rate, supply power consumption for a specific past time interval,
   - next the optimal oscillator output frequency value is predicted for a set future time interval,
   - then the division value for the frequency divider is determined, which is the ratio of the predicted optimal output frequency of the oscillator retuned to the standard oscillator frequency, next the output frequency of the retuned oscillator is checked.

5. Power control system in microprocessor structures containing at least one temperature sensor and a circuit of voltage-controlled oscillator **characterised in that** it has an arbitration unit (AU), connected via a characteristic shaping unit (WSC) and a maximum temperature (MT) selection system to at least one temperature sensor (TS), in addition the arbitration unit (AU) is connected to the retuned oscillator (OSC).
6. The power control system as claimed in claim 5 **characterised in that** it has the arbitration unit (AU), connected to the characteristic forming block (WSC) and the retuned oscillator (OSC), in addition the arbitration unit (AU) is fitted with input circuits for the signal determining the set frequency.
7. The power control system as claimed in claim 5 **characterised in that** it has the prediction unit (PR) which is connected to the temperature measurement unit (TS), the supply current measurement unit (IDD), the past energy consumption measurement unit (ESR), the future predicted energy consumption estimation unit (OS), in addition the prediction unit (PR) is connected to the frequency divider (FD), which in turn is connected to the retuned oscillator (OSC) and the comparison unit (PD/PFD), and this one is

connected to the standard oscillator ($F_0$) and through the forming unit (PD/PFD) to the retuned oscillator (OSC).

8. The power control system as claimed in claim 7 **characterised in that** the comparison unit (PD/PFD) contains the phase detector circuit.
9. The power control system as claimed in claim 7 **characterised in that** the comparison unit (PD/PFD) contains the phase detector and frequency detector circuits.
10. The power control system as claimed in claim 7 **characterised in that** the forming unit (PCP/LPF) has a low-pass filter.
11. The power control system as claimed in claim 7 **characterised in that** the forming unit (PC/LPF) has a charge pump.

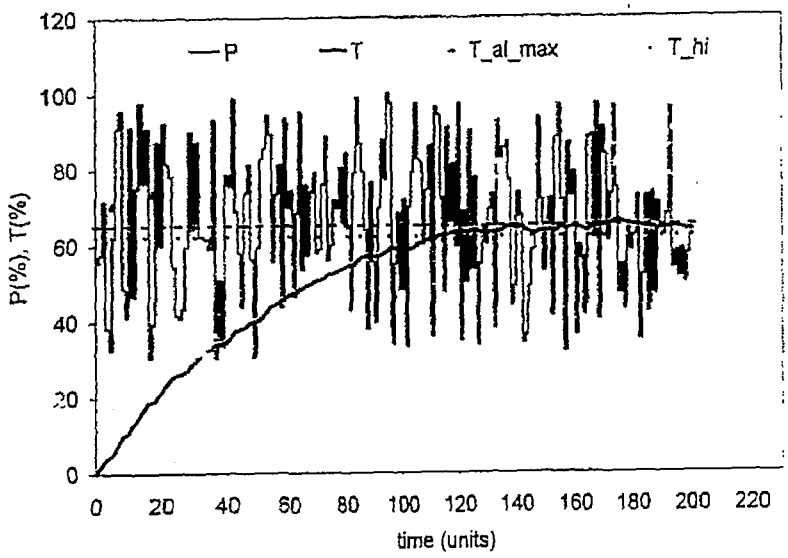
P
T
T_al_max
T_hi
P(%), T(%)
time (units)
0
20
40
60
80
100
120
140
160
180
200
220

Fig.1

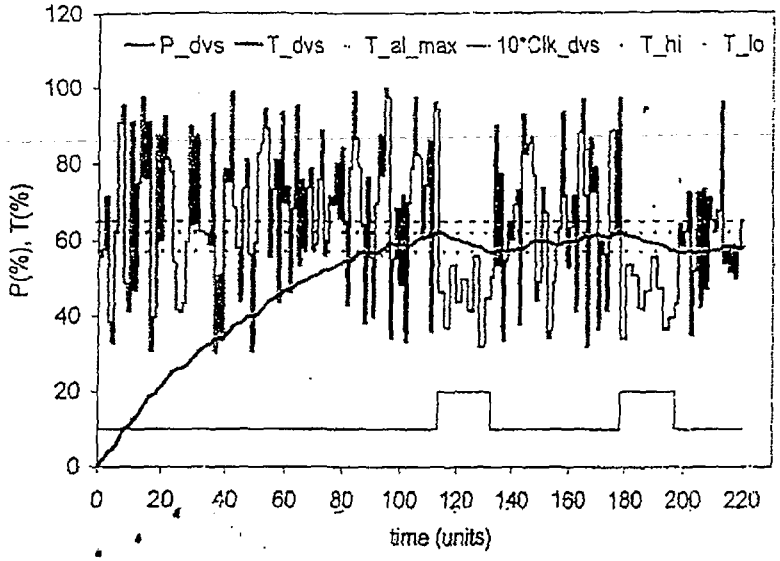
P_dvs
T_dvs
T_al_max
10*Clk_dvs
T_hi
T_lo
P(%), T(%)
time (units)

Fig.2

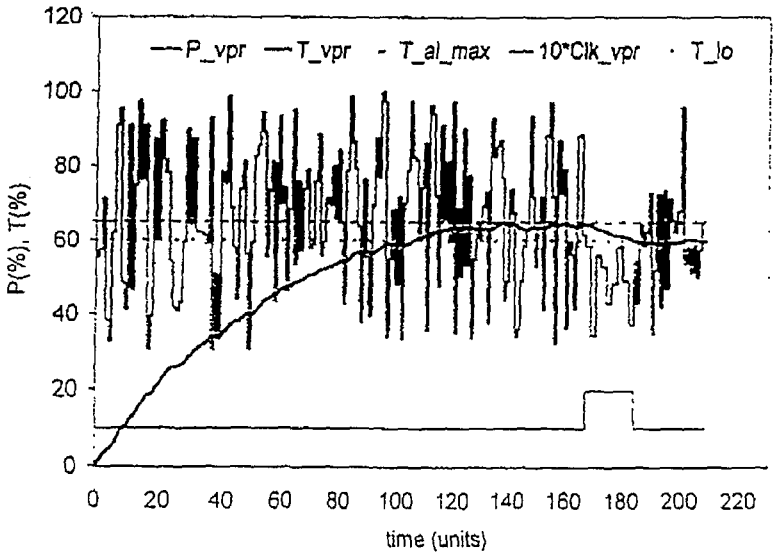
P_vpr
T_vpr
T_al_max
10*Clk_vpr
T_lo
P(%), T(%)
time (units)

Fig.3

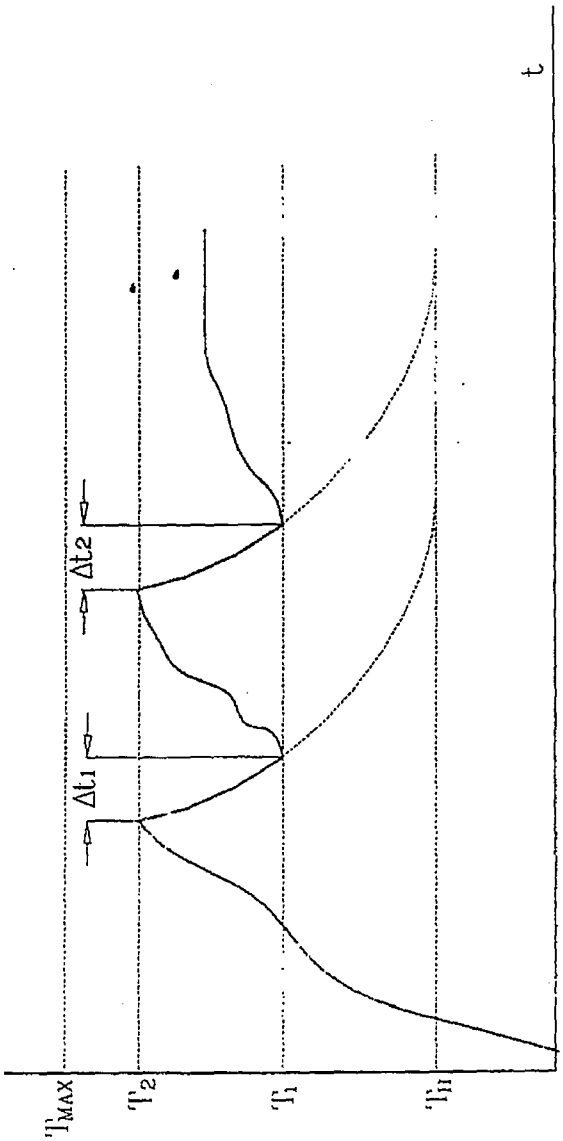


Fig.4

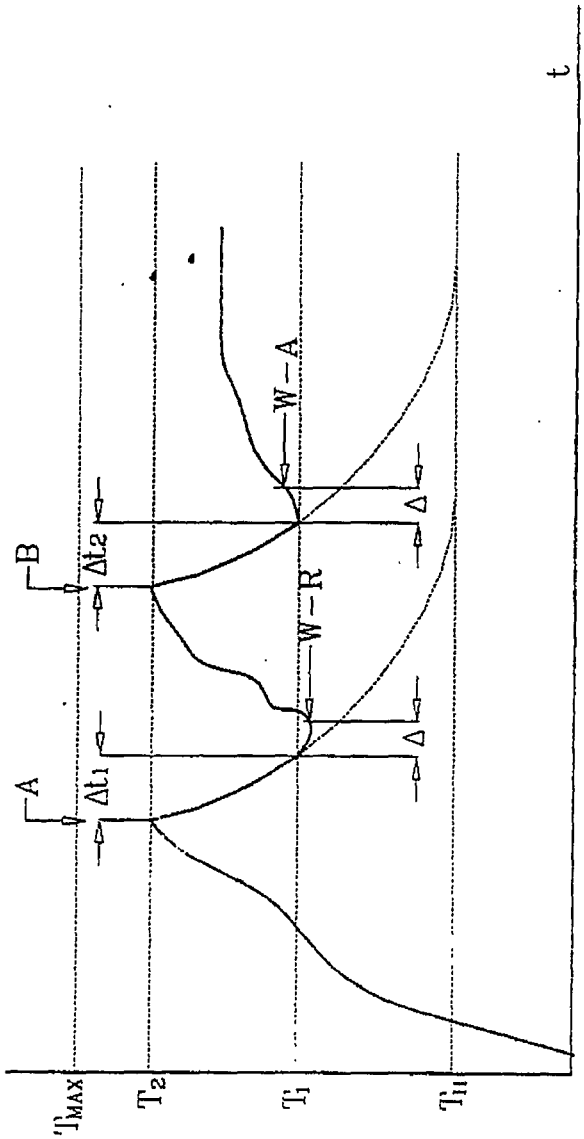


Fig.5

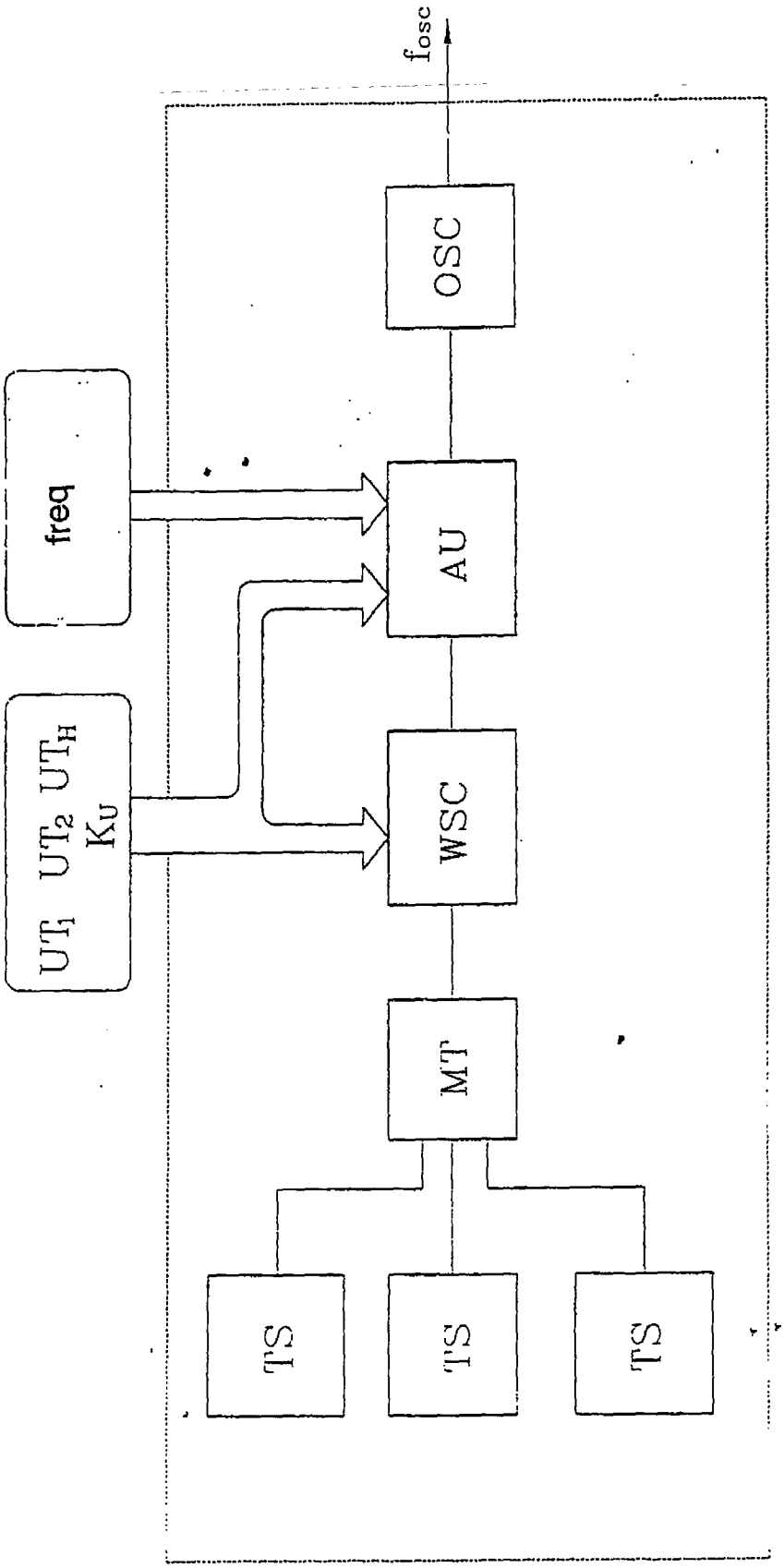


Fig.6

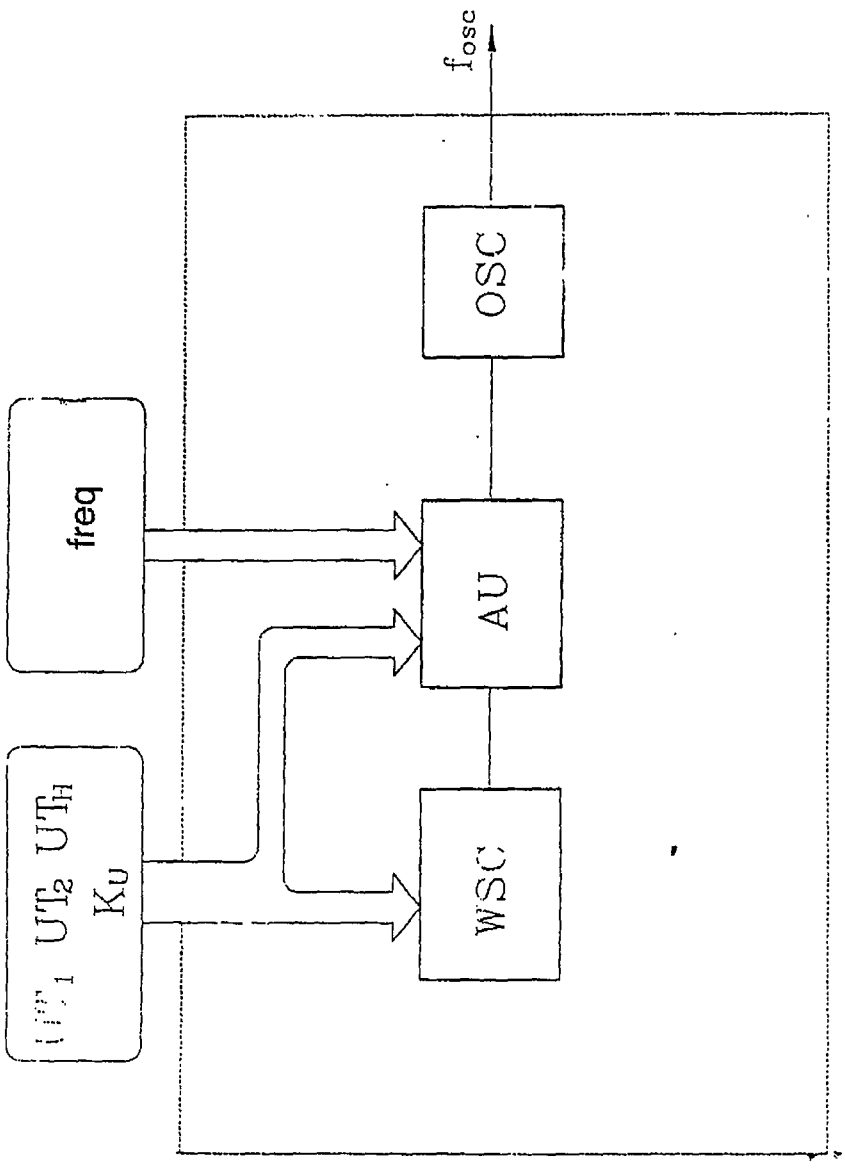


Fig.7

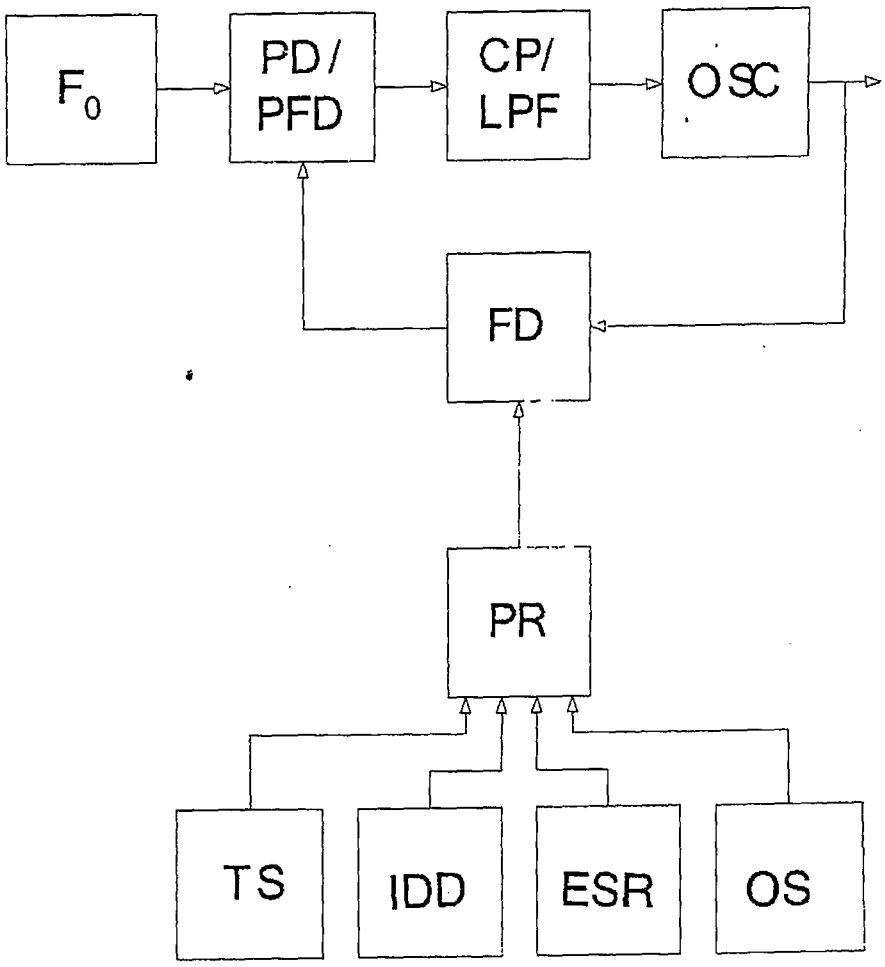


Fig.8

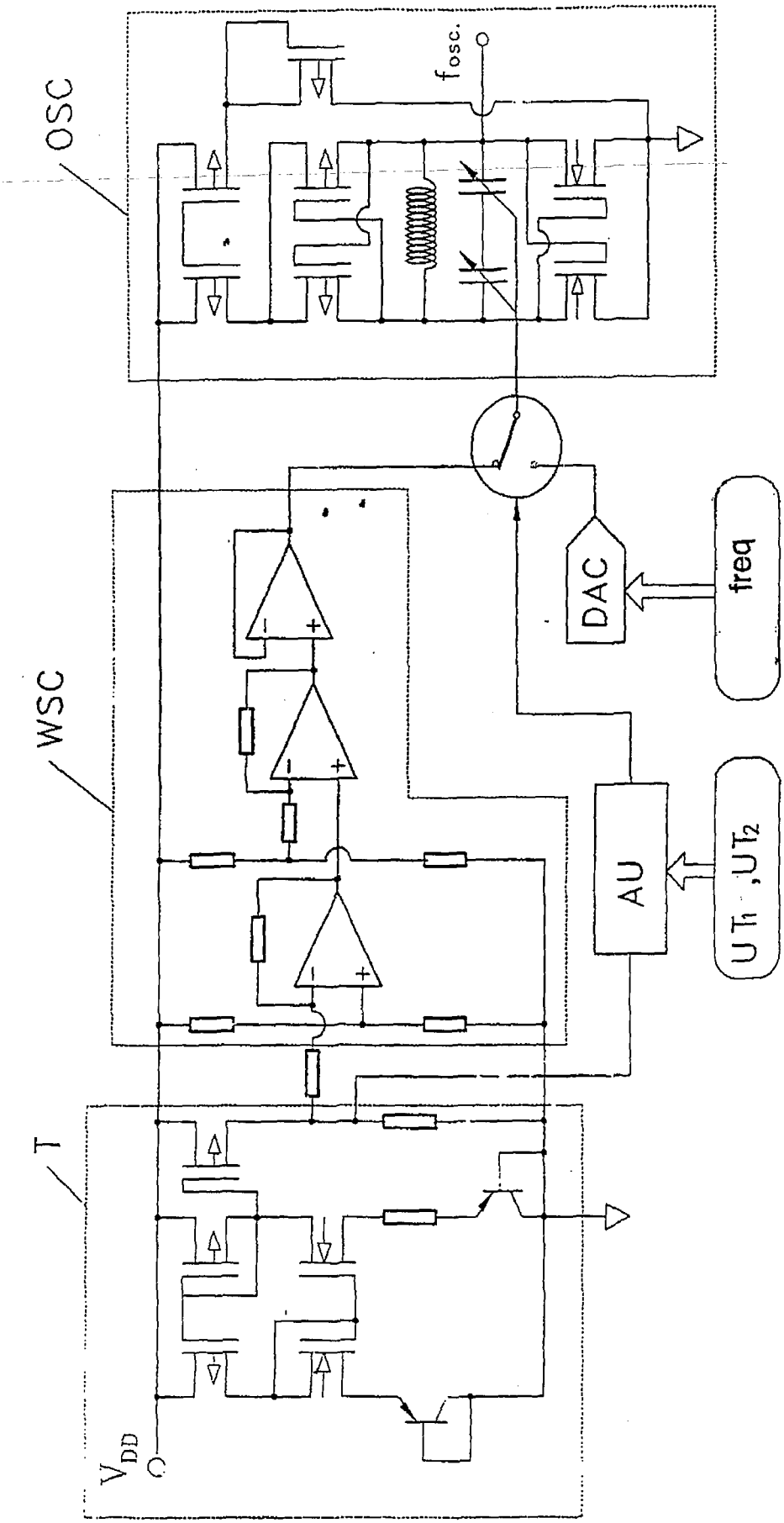


Fig.9

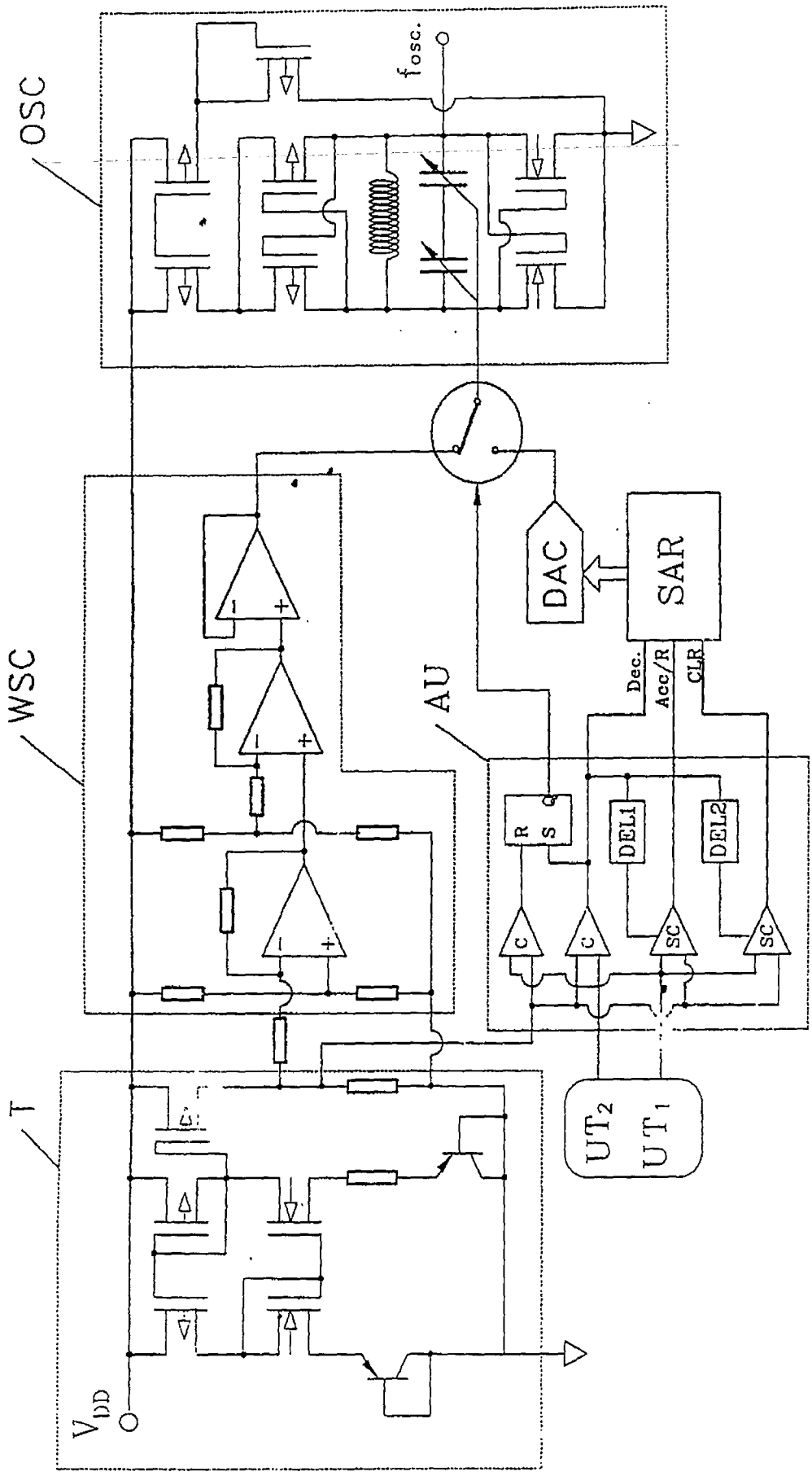
OSC
$f_{osc.}$
WSC
AU
DAC
SAR
Dec.
Acc/R
CLR
R
S
Q
DEL1
DEL2
C
C
SC
SC
T
$UT_2$
$UT_1$
$V_{DD}$

Fig.10

# INTERNATIONAL SEARCH REPORT

International application No
PCT/PL2010/050050

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F1/20
ADD. G06F1/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
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| X | US 5 451 892 A (BAILEY JOSEPH A [US]) 19 September 1995 (1995-09-19) column 8, line 1 - line 32; figures 1,2 | 1-11 |
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 21 February 2011 | 01/03/2011 |

| Name and mailing address of the ISA/ | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040,<br>Fax: (+31-70) 340-3016 | Anastassiades, G |

# INTERNATIONAL SEARCH REPORT

International application No
PCT/PL2010/050050

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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