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(54) **EDGELESS LARGE AREA CAMERA SYSTEM**

(71) Applicant: **Fermi Research Alliance, LLC**, Batavia, IL (US)

(72) Inventors: **Farah Fahim**, Glen Ellyn, IL (US); **Grzegorz W. Deptuch**, Forest Park, IL (US); **Pawel Grybos**, Rzaska (PL); **Robert Szczygiel**, Krakow (PL); **Piotr Maj**, Krakow (PL); **Piotr Kmon**, Niepolomice (PL); **David Peter Siddons**, Cutchogue, NY (US); **Joseph Mead**, Manorville, NY (US); **Abdul Khader Rumaiz**, Nesconset, NY (US); **Robert Kent Bradford**, Aurora, IL (US); **John Thomas Weizeorick, III**, Naperville, IL (US)

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(51) **Int. Cl.**

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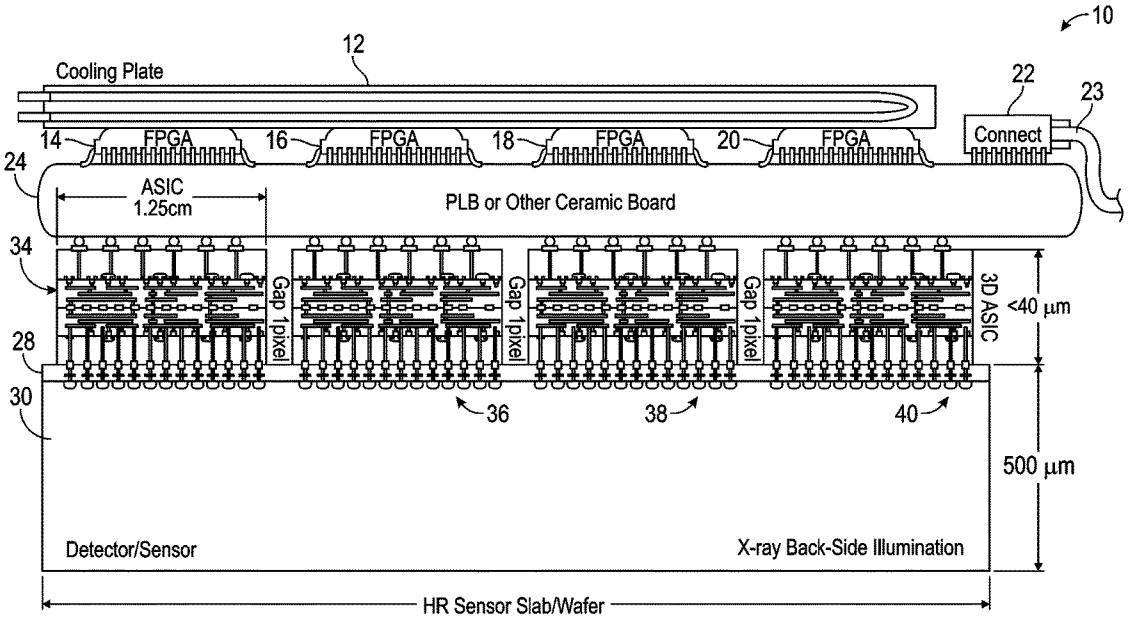
H04N 5/32	(2006.01)
H04N 5/378	(2006.01)

(52) **U.S. Cl.**

CPC ***H04N 5/3696*** (2013.01); ***H04N 5/378*** (2013.01); ***H04N 5/32*** (2013.01)

(57) **ABSTRACT**

A detecting apparatus includes a multi-tier 3D integrated ASIC comprising one or more analog tiers and one or more digital tiers, and a sensor bonded to the multi-tier 3D integrated ASIC. The detecting apparatus includes an electrical substrate and a group of FPGAs or custom data management ASICs. The detecting apparatus also includes a thermal management system, a power distribution system and one or more connectors to transfer data to a data acquisition system configured for radiation spectroscopy or imaging with zero suppressed or full frame readout.



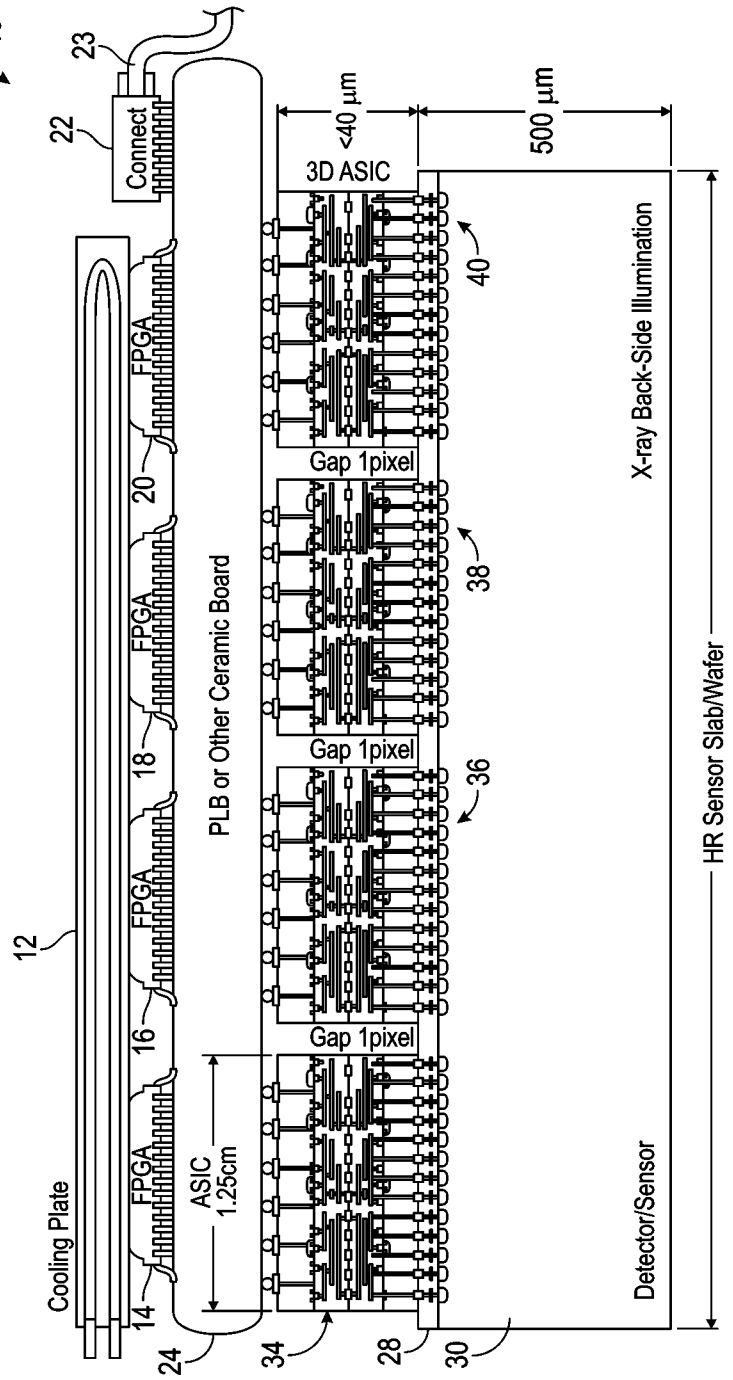

10
23
22
Connect
<40 µm
500 µm
3D ASIC
40
FPGA
20
Gap 1pixel
X-ray Back-Side Illumination
38
FPGA
18
PLB or Other Ceramic Board
Gap 1pixel
36
FPGA
12
16
Gap 1pixel
ASIC
1.25cm
HR Sensor Slab/Wafer
Cooling Plate
FPGA
14
Detector/Sensor
24
34
28
30

FIG. 1

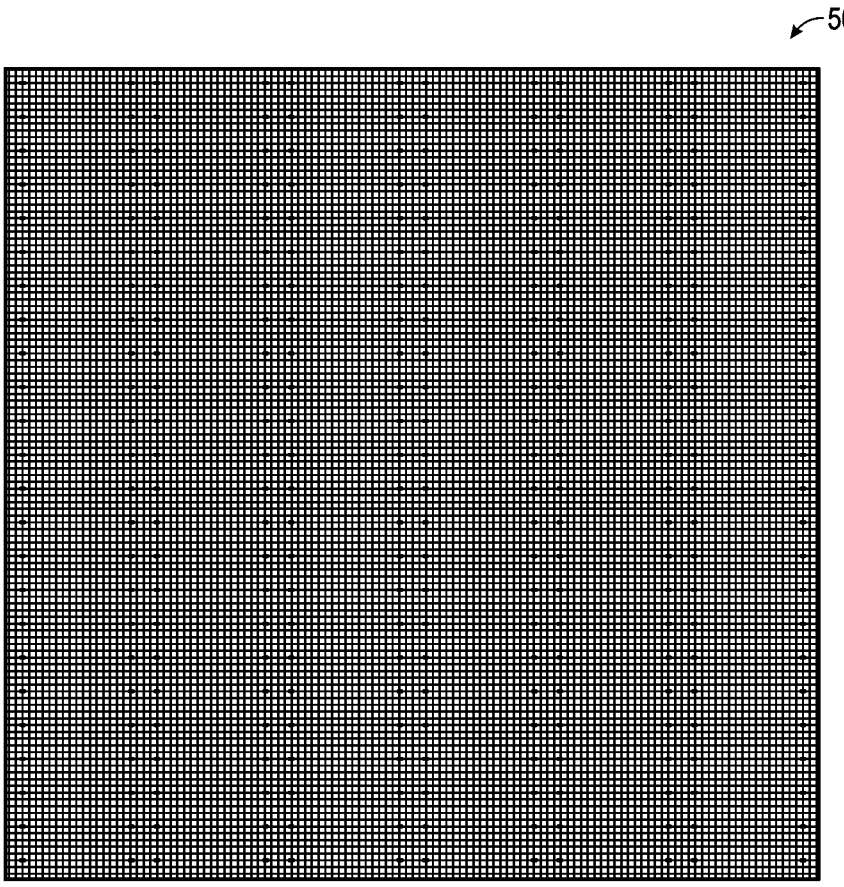


FIG. 2

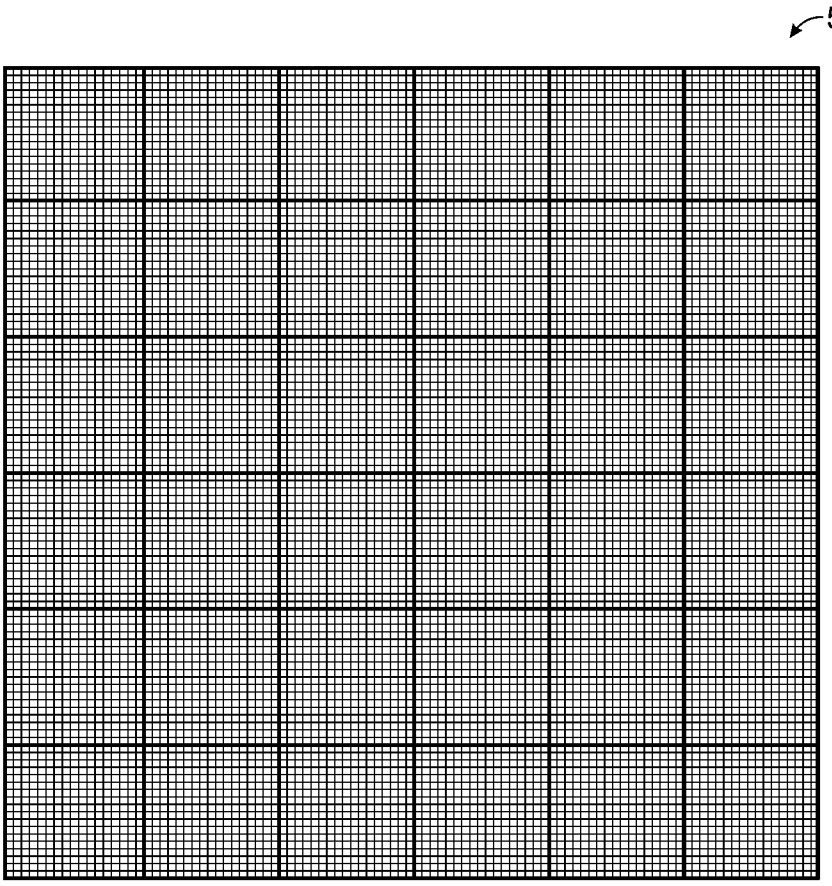


FIG. 3

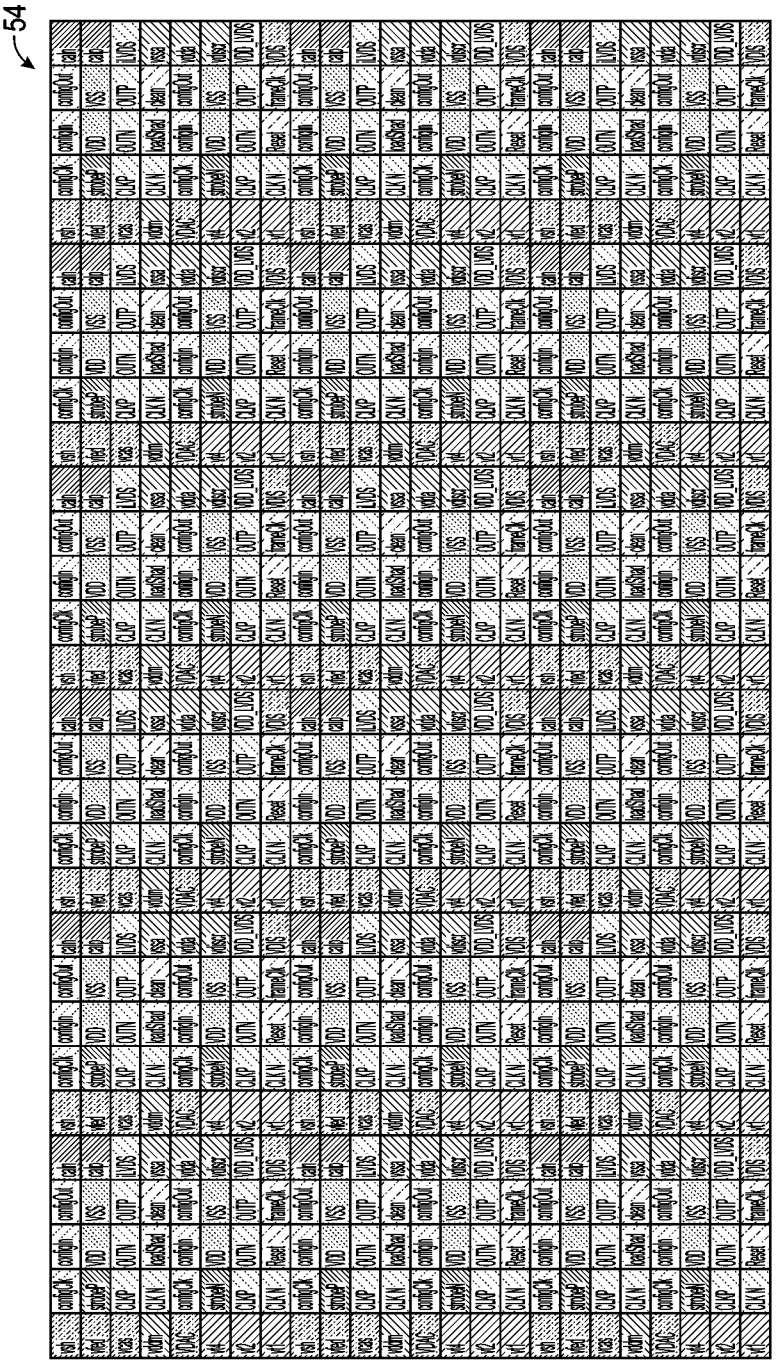


FIG. 4

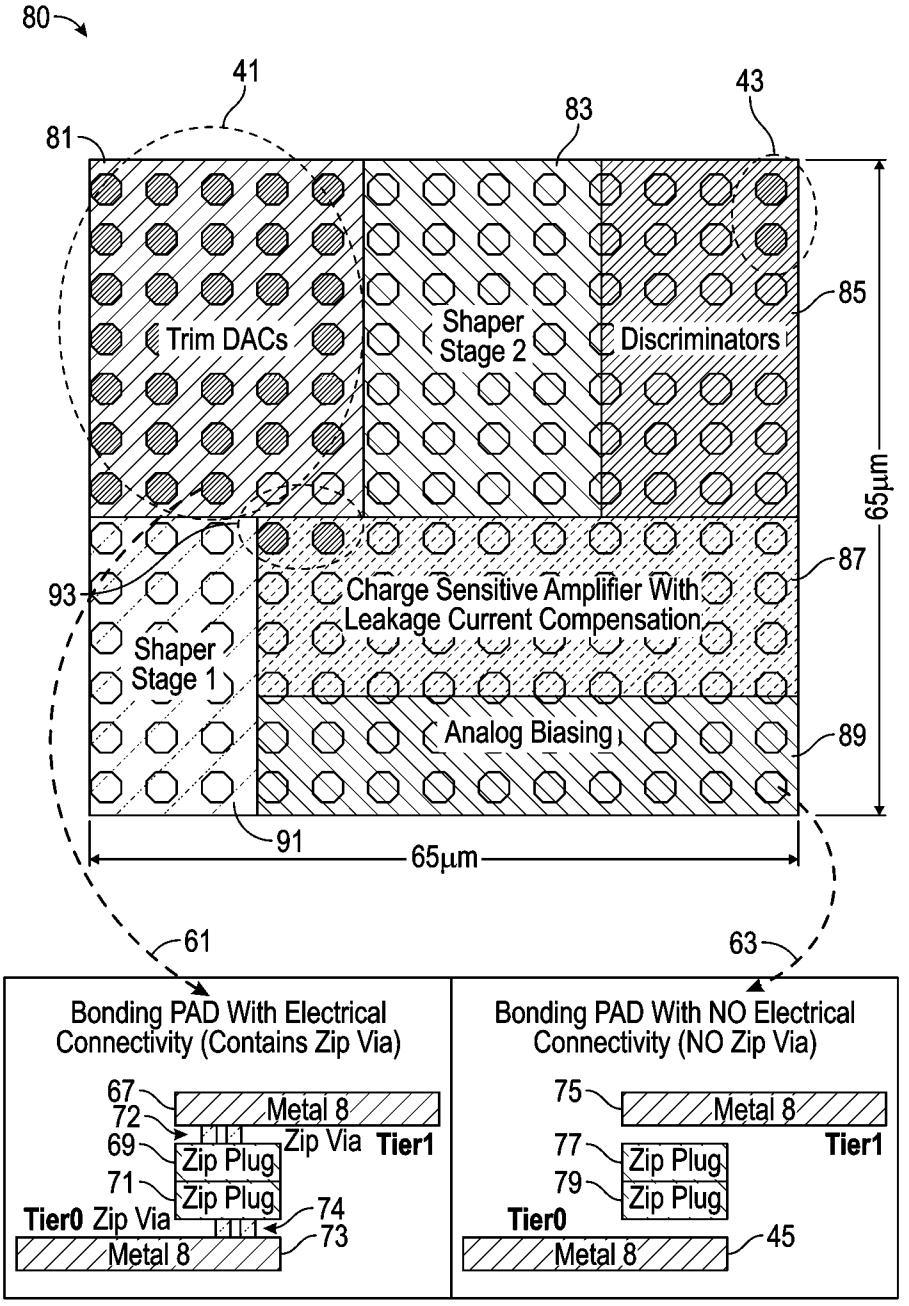

80
41
43
81
83
85
Trim DACs
Shaper Stage 2
Discriminators
65µm
87
93
Charge Sensitive Amplifier With Leakage Current Compensation
Shaper Stage 1
89
Analog Biasing
91
65µm
61
63
Bonding PAD With Electrical Connectivity (Contains Zip Via)
Bonding PAD With NO Electrical Connectivity (NO Zip Via)
67
72
Metal 8
Zip Via
Tier1
69
Zip Plug
71
Zip Plug
Tier0 Zip Via
74
73
Metal 8
75
Metal 8
Tier1
77
Zip Plug
79
Zip Plug
Tier0
Metal 8
45

FIG. 5

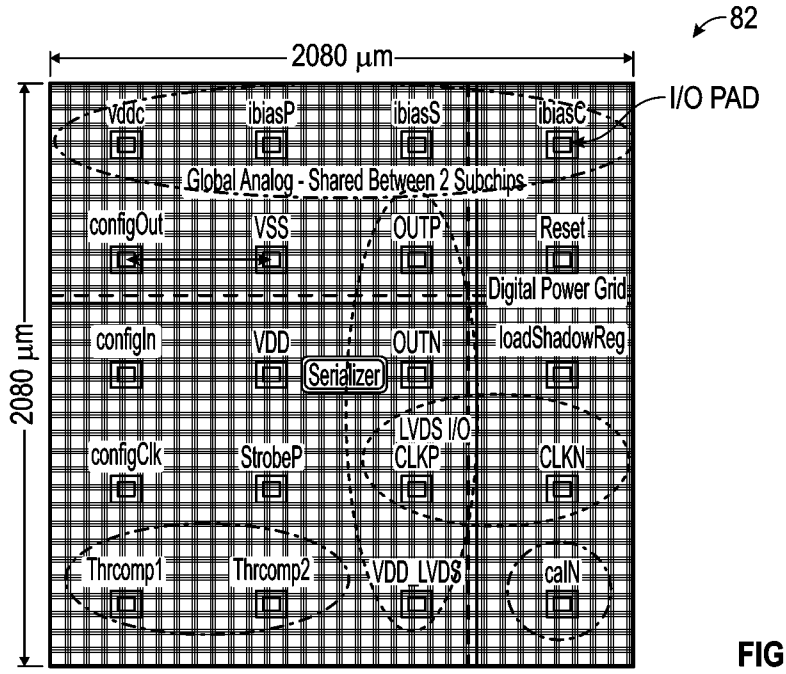

82
2080 µm
2080 µm
I/O PAD
vddc
ibiasP
ibiasS
ibiasC
Global Analog - Shared Between 2 Subchips
configOut
VSS
OUTP
Reset
Digital Power Grid
configIn
VDD
OUTN
loadShadowReg
Serializer
LVDS I/O
configClk
StrobeP
CLKP
CLKN
Thrcomp1
Thrcomp2
VDD_LVDS
calN

FIG. 6

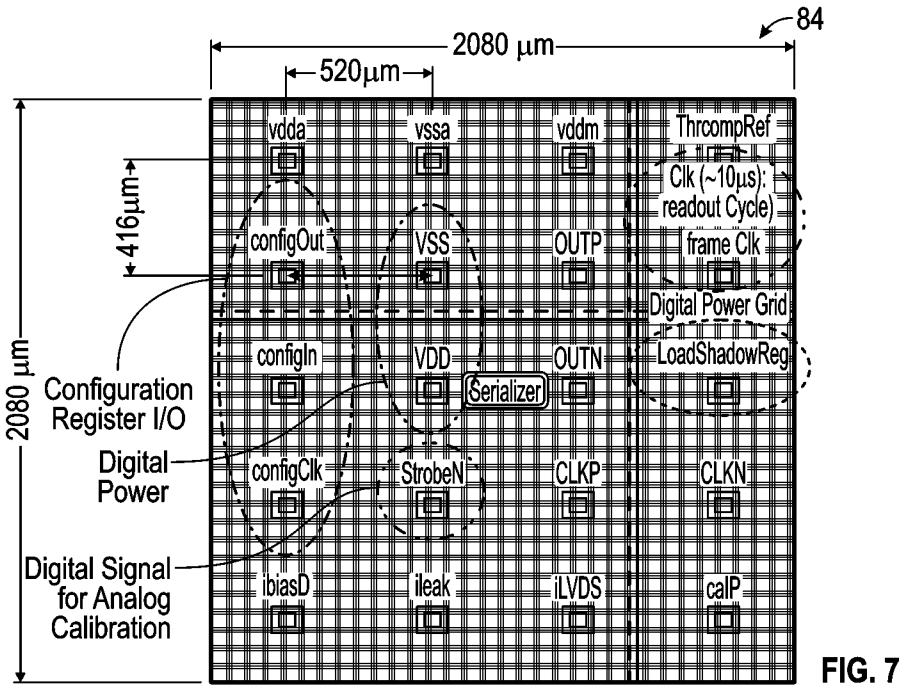

84
2080 µm
520µm
416µm
2080 µm
vdda
vssa
vddm
ThrcompRef
Clk (~10µs): readout Cycle)
configOut
VSS
OUTP
frame Clk
Digital Power Grid
configIn
VDD
OUTN
LoadShadowReg
Serializer
Configuration Register I/O
Digital Power
configClk
StrobeN
CLKP
CLKN
Digital Signal for Analog Calibration
ibiasD
ileak
iLVDS
calP

FIG. 7

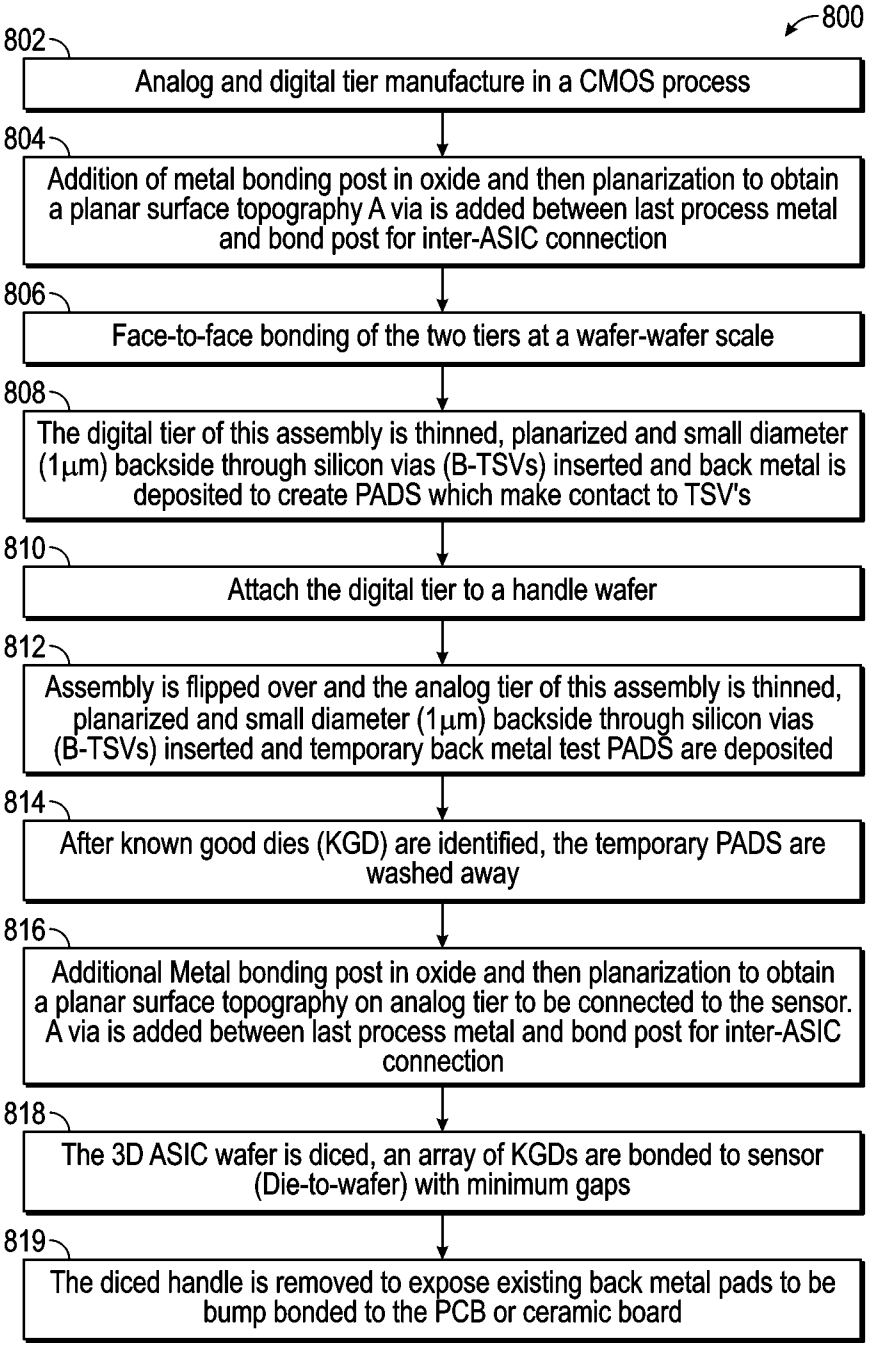

800
802
Analog and digital tier manufacture in a CMOS process
804
Addition of metal bonding post in oxide and then planarization to obtain a planar surface topography A via is added between last process metal and bond post for inter-ASIC connection
806
Face-to-face bonding of the two tiers at a wafer-wafer scale
808
The digital tier of this assembly is thinned, planarized and small diameter (1μm) backside through silicon vias (B-TSVs) inserted and back metal is deposited to create PADS which make contact to TSV's
810
Attach the digital tier to a handle wafer
812
Assembly is flipped over and the analog tier of this assembly is thinned, planarized and small diameter (1μm) backside through silicon vias (B-TSVs) inserted and temporary back metal test PADS are deposited
814
After known good dies (KGD) are identified, the temporary PADS are washed away
816
Additional Metal bonding post in oxide and then planarization to obtain a planar surface topography on analog tier to be connected to the sensor. A via is added between last process metal and bond post for inter-ASIC connection
818
The 3D ASIC wafer is diced, an array of KGDs are bonded to sensor (Die-to-wafer) with minimum gaps
819
The diced handle is removed to expose existing back metal pads to be bump bonded to the PCB or ceramic board

FIG. 8

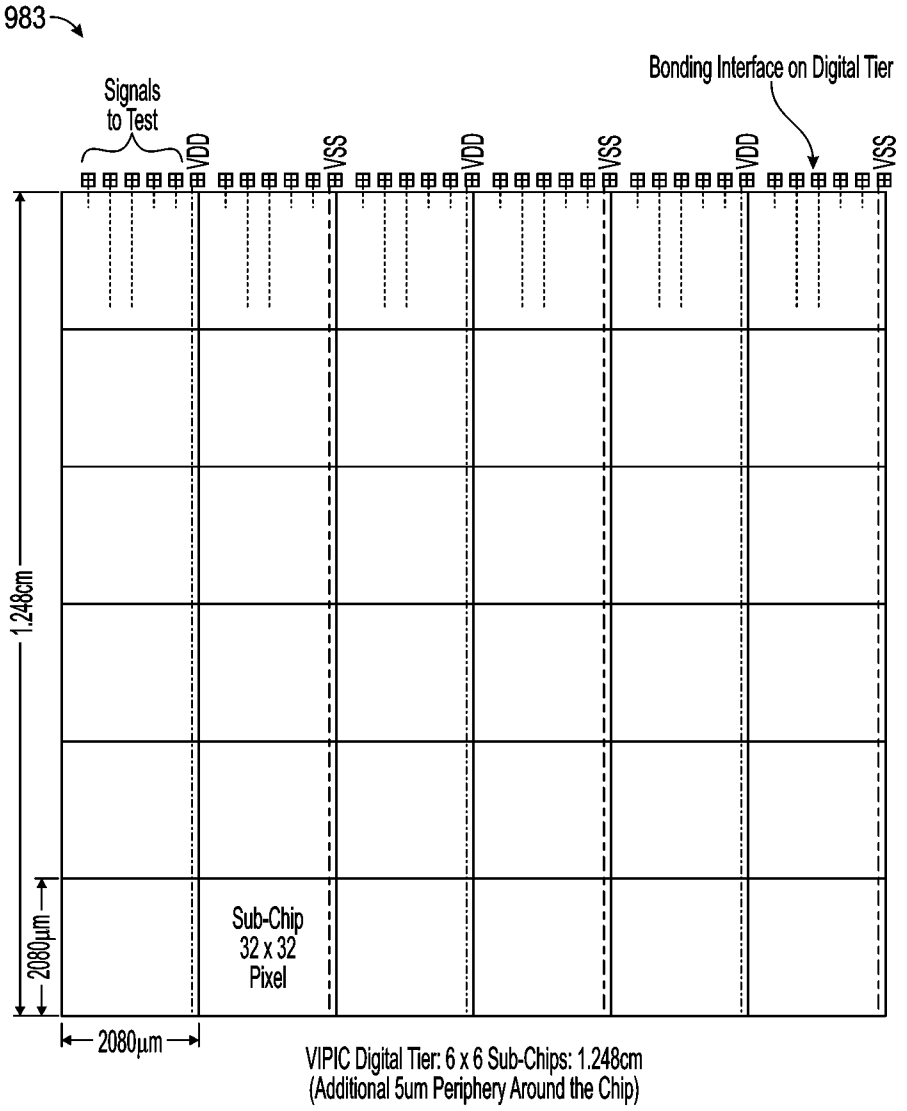

983
Signals to Test
VDD
VSS
VDD
VSS
VDD
VSS
Bonding Interface on Digital Tier
1.248cm
2080μm
Sub-Chip 32 x 32 Pixel
2080μm
VIPIC Digital Tier: 6 x 6 Sub-Chips: 1.248cm
(Additional 5um Periphery Around the Chip)

FIG. 9A

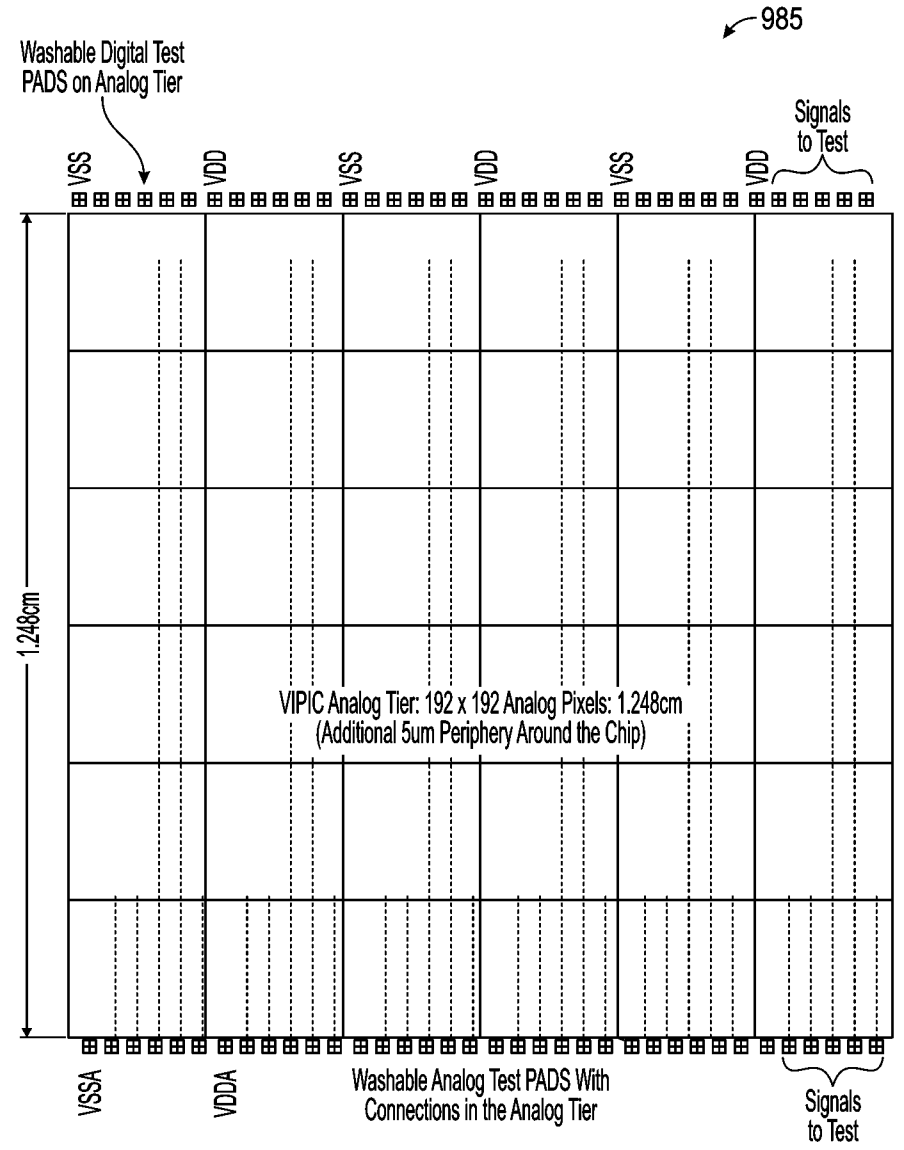

985
Washable Digital Test PADS on Analog Tier
Signals to Test
VSS
VDD
VSS
VDD
VSS
VDD
1.248cm
VIPIC Analog Tier: 192 x 192 Analog Pixels: 1.248cm
(Additional 5um Periphery Around the Chip)
VSSA
VDDA
Washable Analog Test PADS With Connections in the Analog Tier
Signals to Test

FIG. 9B

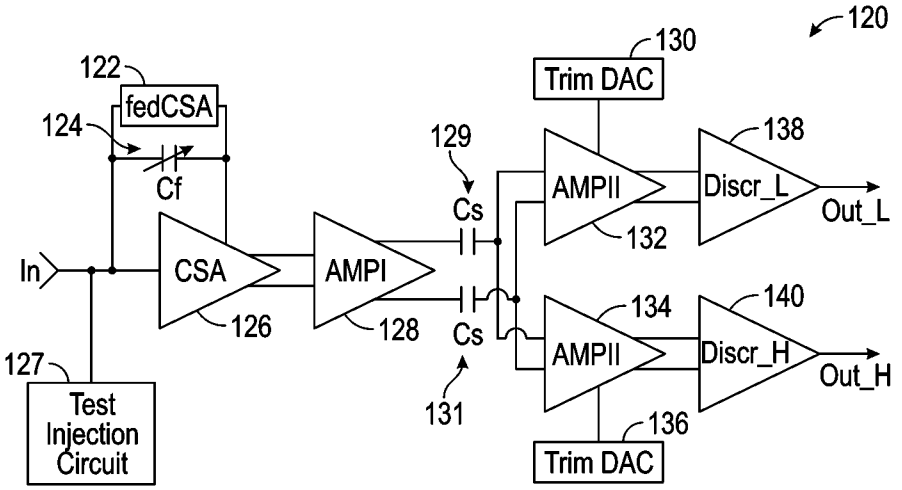

120
130
Trim DAC
122
fedCSA
124
Cf
129
Cs
AMPII
138
Discr_L
Out_L
132
In
CSA
AMPI
126
128
Cs
134
140
AMPII
Discr_H
Out_H
127
Test Injection Circuit
131
136
Trim DAC

FIG. 10

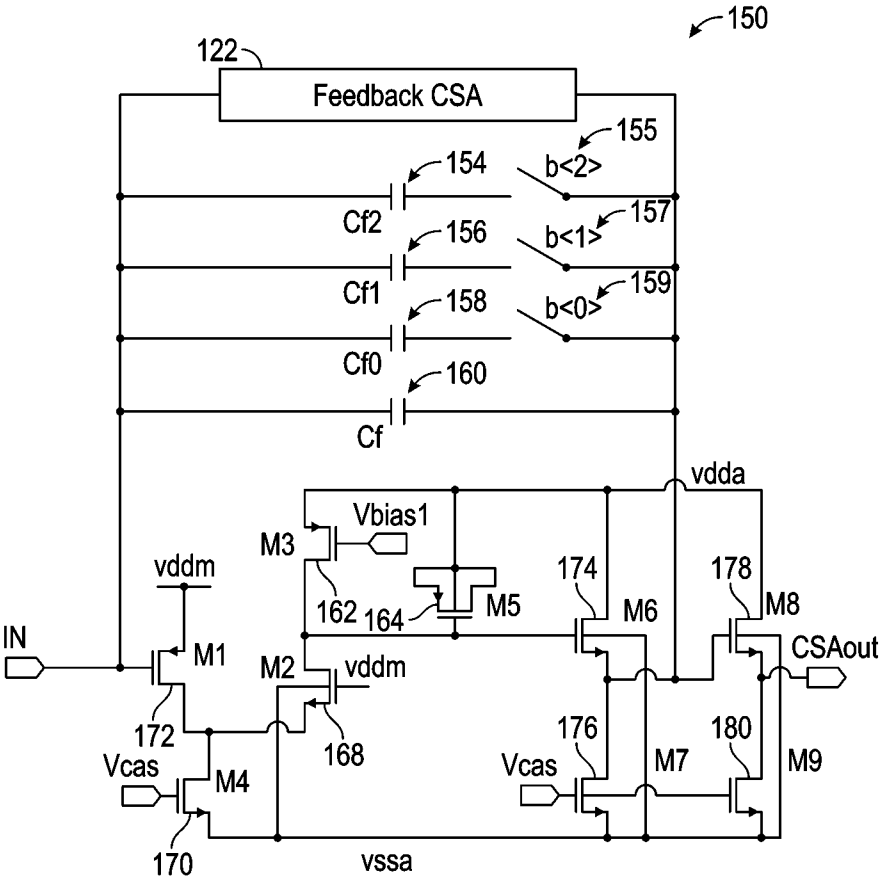

150
122
Feedback CSA
155
154
b<2>
Cf2
157
156
b<1>
Cf1
159
158
b<0>
Cf0
160
Cf
vdda
Vbias1
M3
vddm
174
178
162
164
M5
M6
M8
IN
M1
M2
vddm
CSAout
172
168
176
180
Vcas
M4
Vcas
M7
M9
170
vssa

FIG. 11

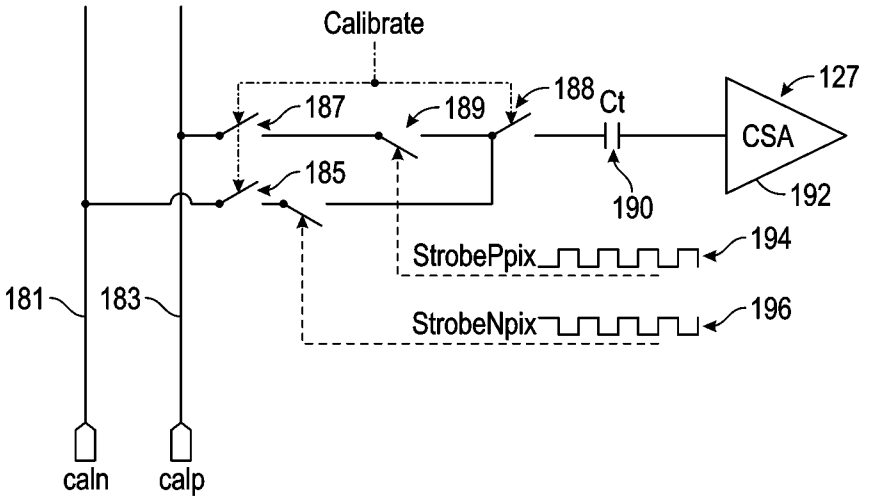

Calibrate
187
189
188
Ct
127
CSA
185
190
192
StrobePpix
194
181
183
StrobeNpix
196
caln
calp

FIG. 12

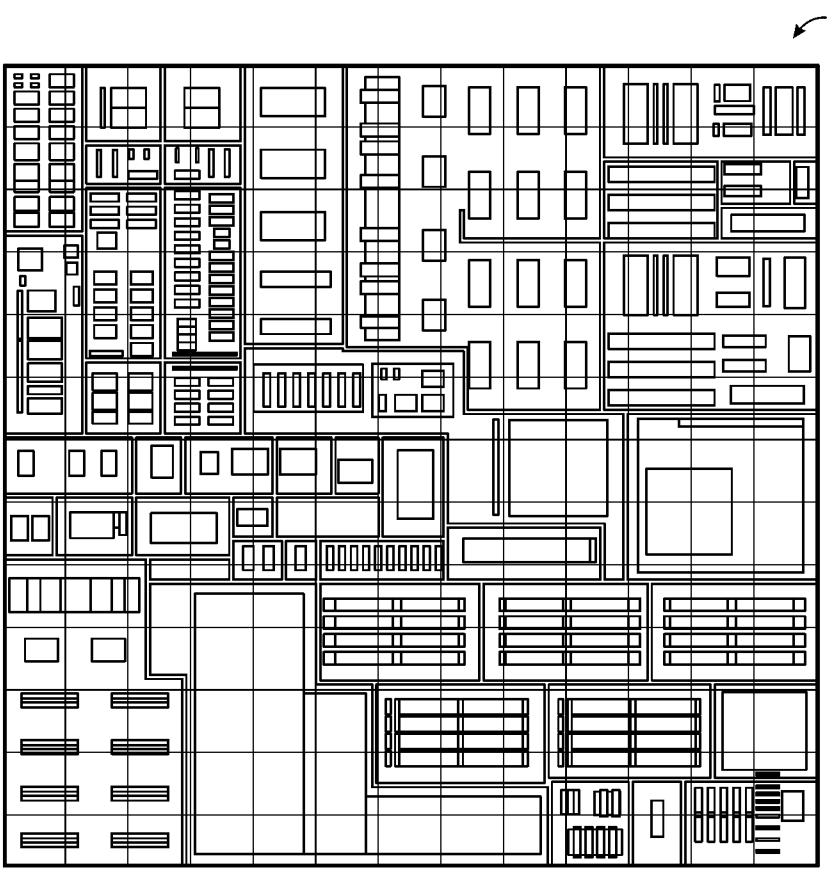


FIG. 13

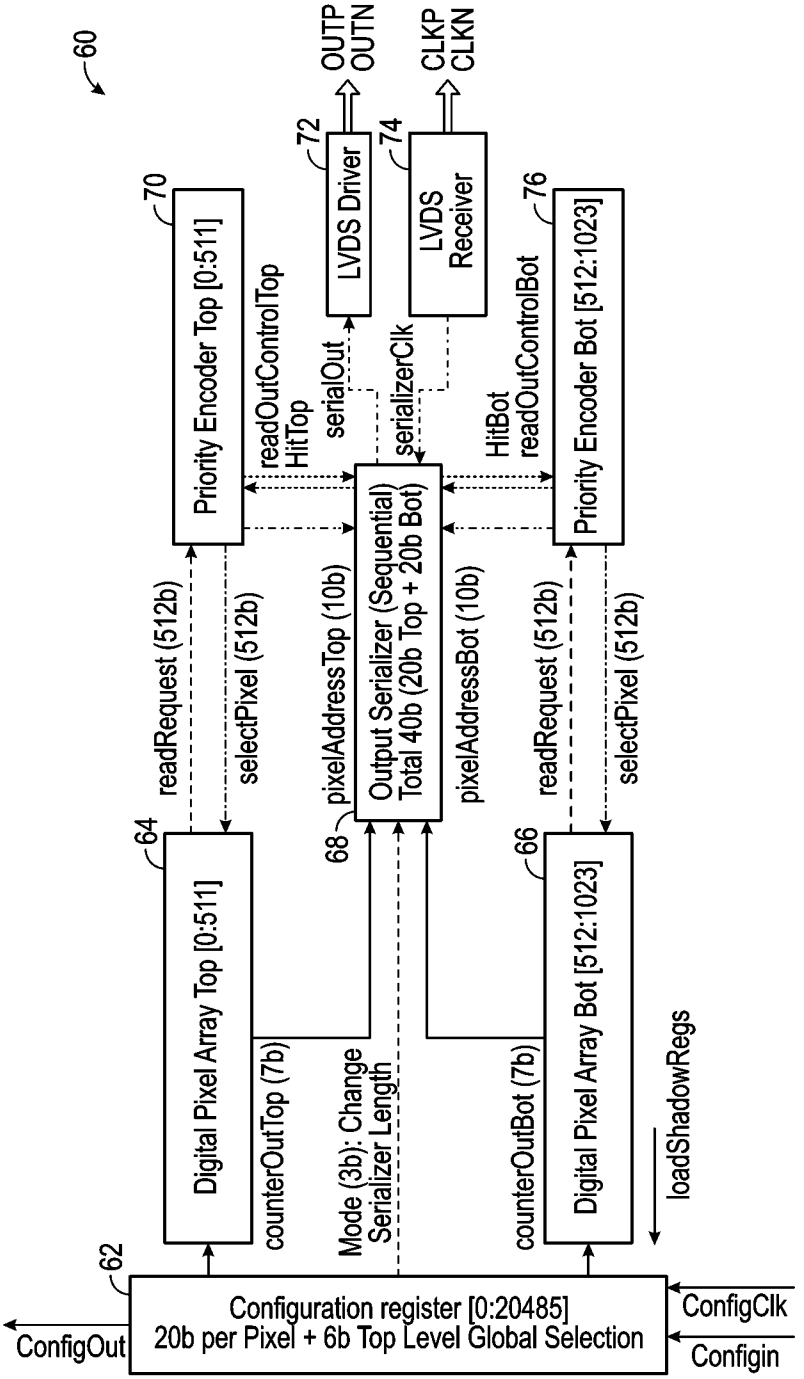

60
OUTP
OUTN
CLKP
CLKN
72
74
LVDS Driver
LVDS Receiver
70
76
Priority Encoder Top [0:511]
Priority Encoder Bot [512:1023]
readOutControlTop
HitTop
serialOut
serializerClk
HitBot
readOutControlBot
readRequest (512b)
selectPixel (512b)
pixelAddressTop (10b)
Output Serializer (Sequential)
Total 40b (20b Top + 20b Bot)
pixelAddressBot (10b)
readRequest (512b)
selectPixel (512b)
64
68
66
Digital Pixel Array Top [0:511]
Digital Pixel Array Bot [512:1023]
counterOutTop (7b)
Mode (3b): Change
Serializer Length
counterOutBot (7b)
loadShadowRegs
62
Configuration register [0:20485]
20b per Pixel + 6b Top Level Global Selection
ConfigOut
ConfigClk
Configin

FIG. 14

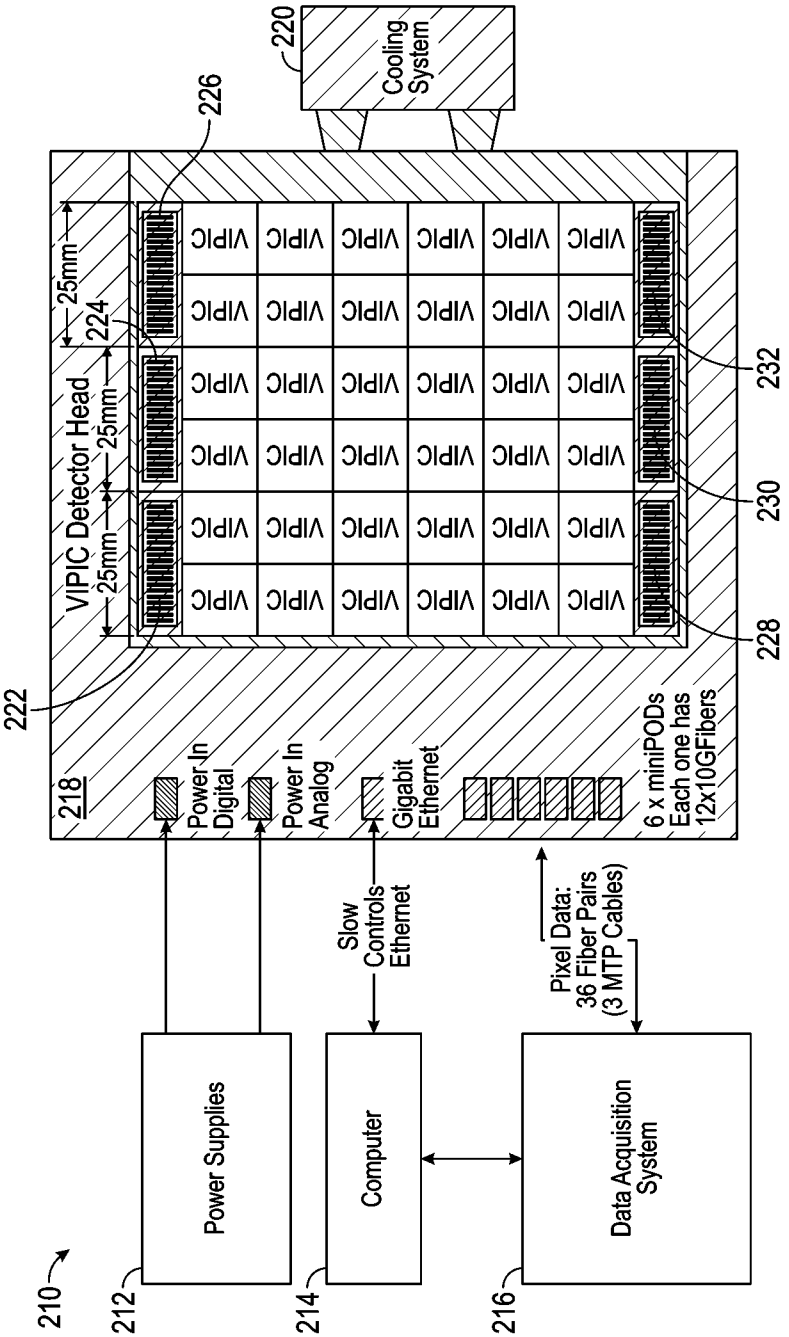

220
Cooling System
226
VIPIC Detector Head
25mm
25mm
25mm
224
222
218
232
230
228
Power In Digital
Power In Analog
Gigabit Ethernet
6 x miniPODs Each one has 12x10GFibers
Slow Controls Ethernet
Pixel Data: 36 Fiber Pairs (3 MTP Cables)
Power Supplies
Computer
Data Acquisition System
210
212
214
216

FIG. 15

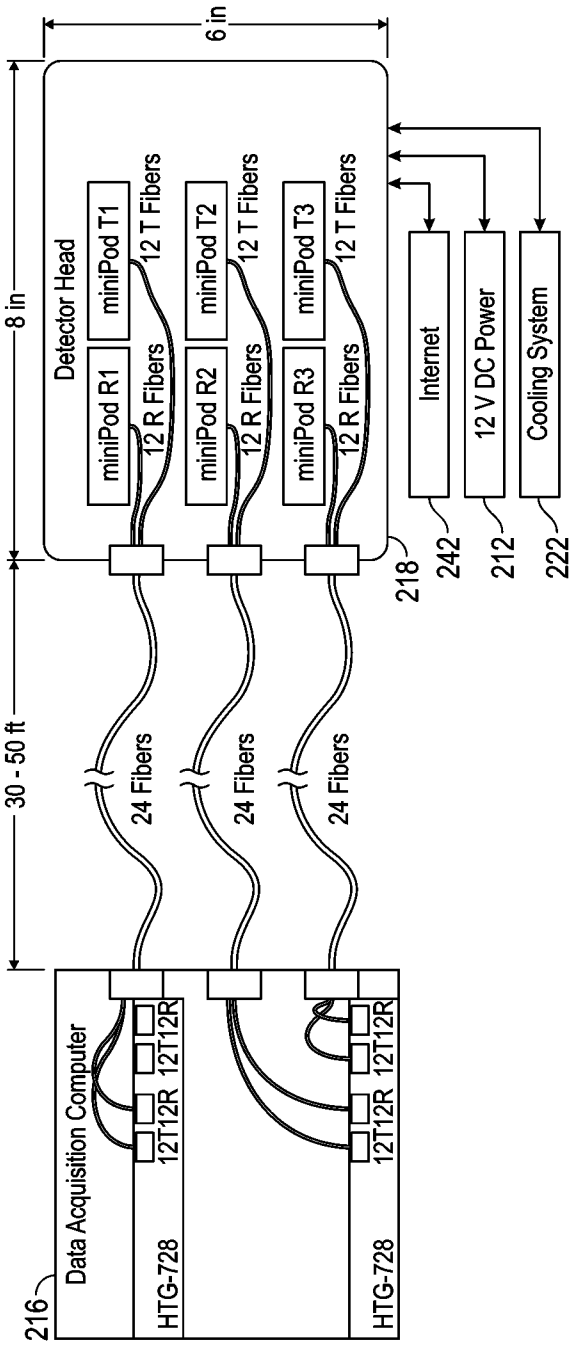

6 in
8 in
30 - 50 ft
Detector Head
miniPod T1
miniPod T2
miniPod T3
miniPod R1
miniPod R2
miniPod R3
12 T Fibers
12 R Fibers
24 Fibers
Internet
12 V DC Power
Cooling System
218
242
212
222
216
Data Acquisition Computer
HTG-728
12T12R

FIG. 16

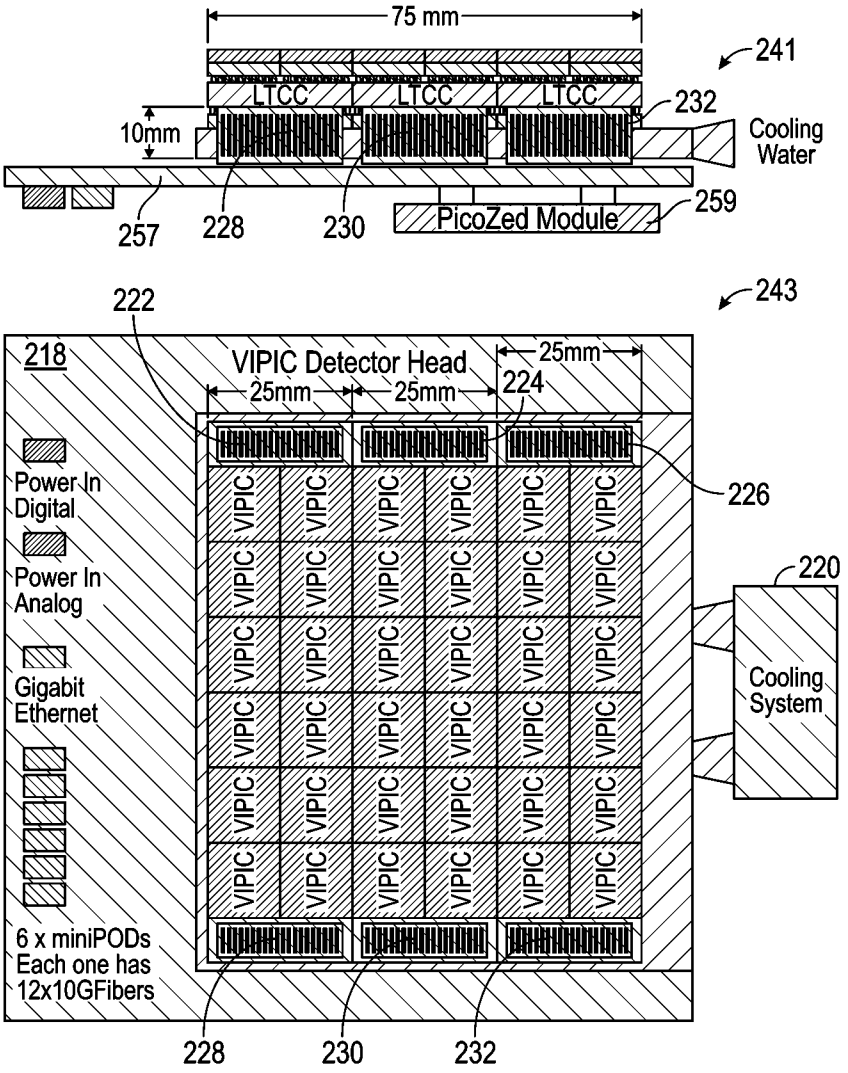

75 mm
241
LTCC
LTCC
LTCC
232
10mm
Cooling Water
259
PicoZed Module
257
228
230
243
222
218
VIPIC Detector Head
25mm
25mm
25mm
224
226
220
Power In Digital
Power In Analog
Gigabit Ethernet
6 x miniPODs Each one has 12x10GFibers
Cooling System
VIPIC
228
230
232

FIG. 17

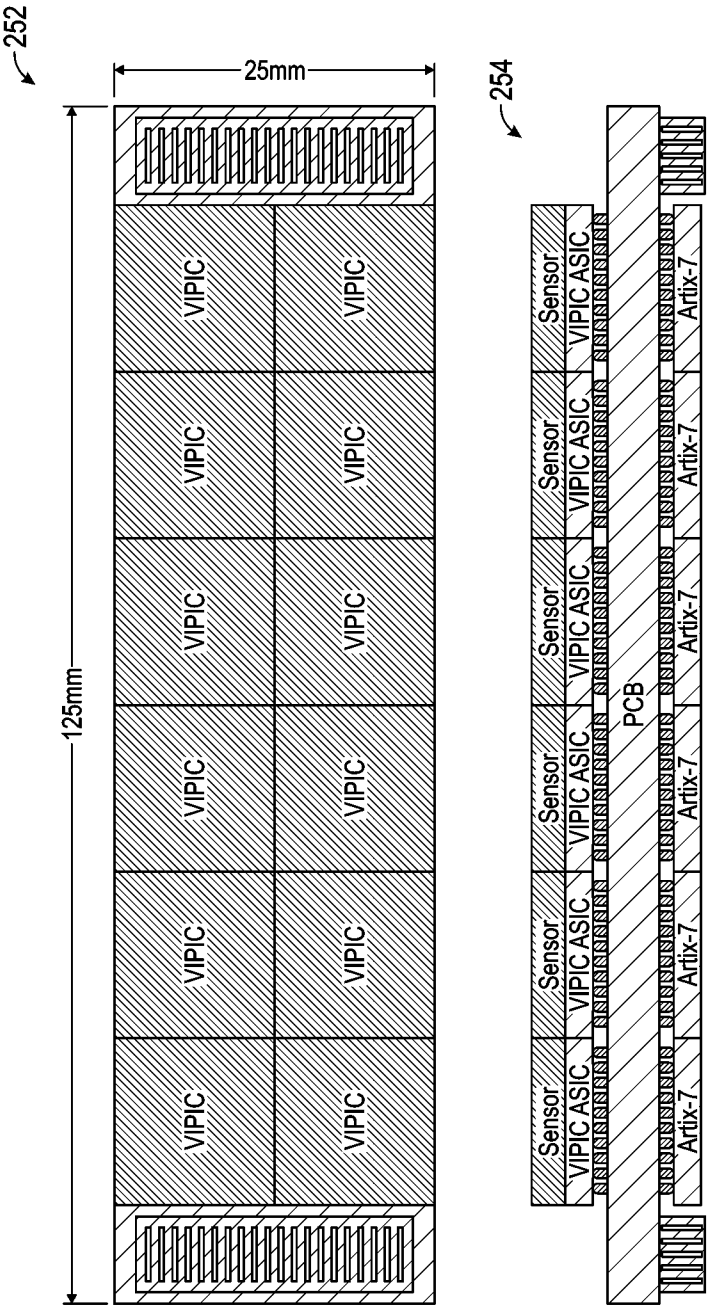


FIG. 18

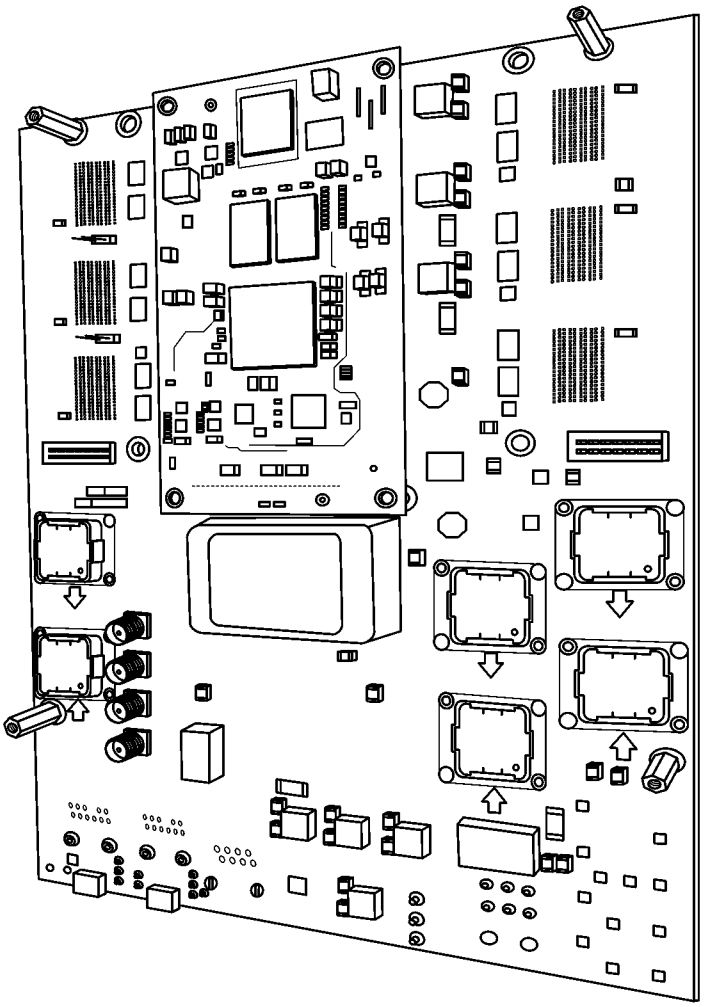


FIG. 19

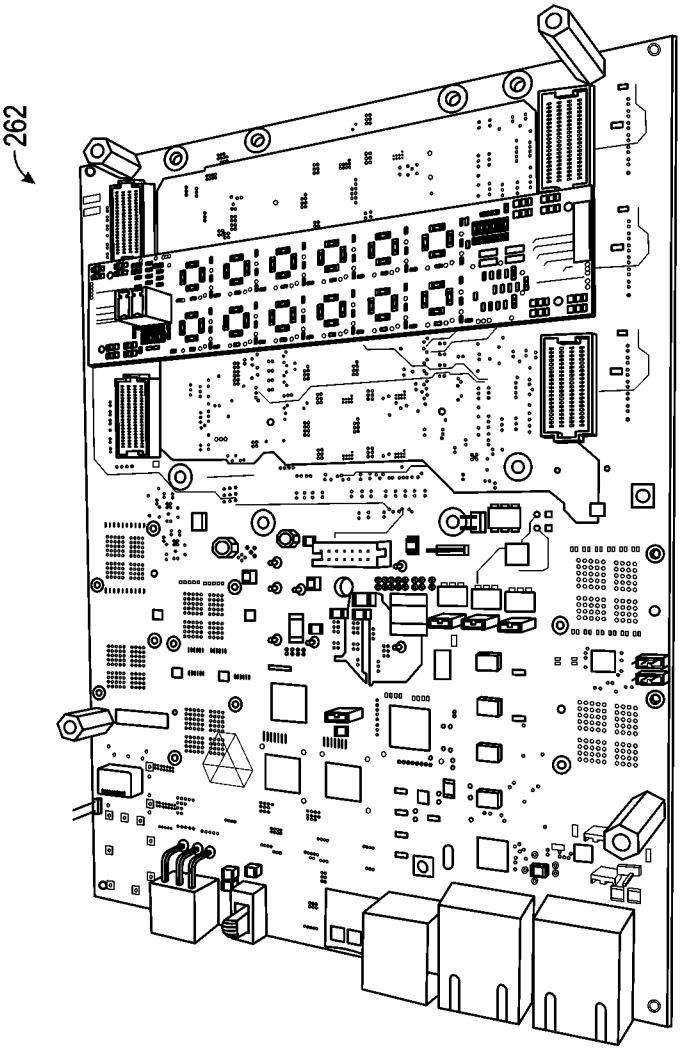


FIG. 20

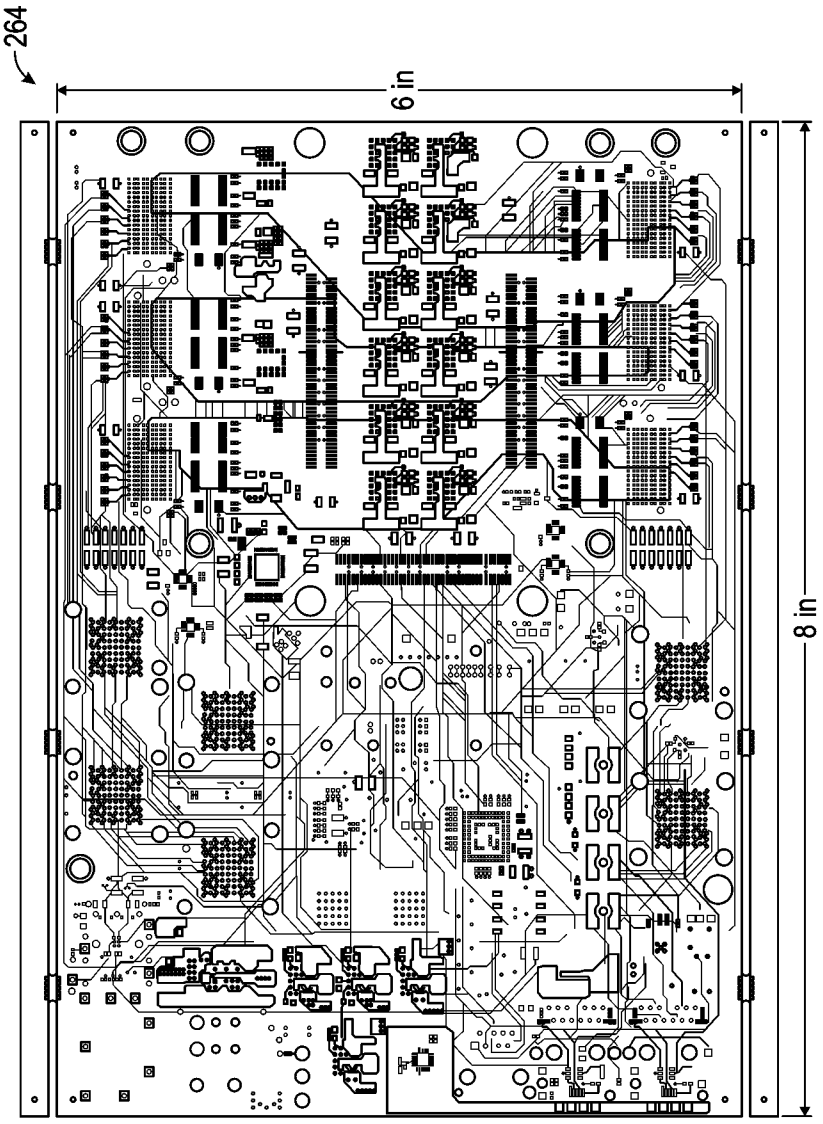


FIG. 21

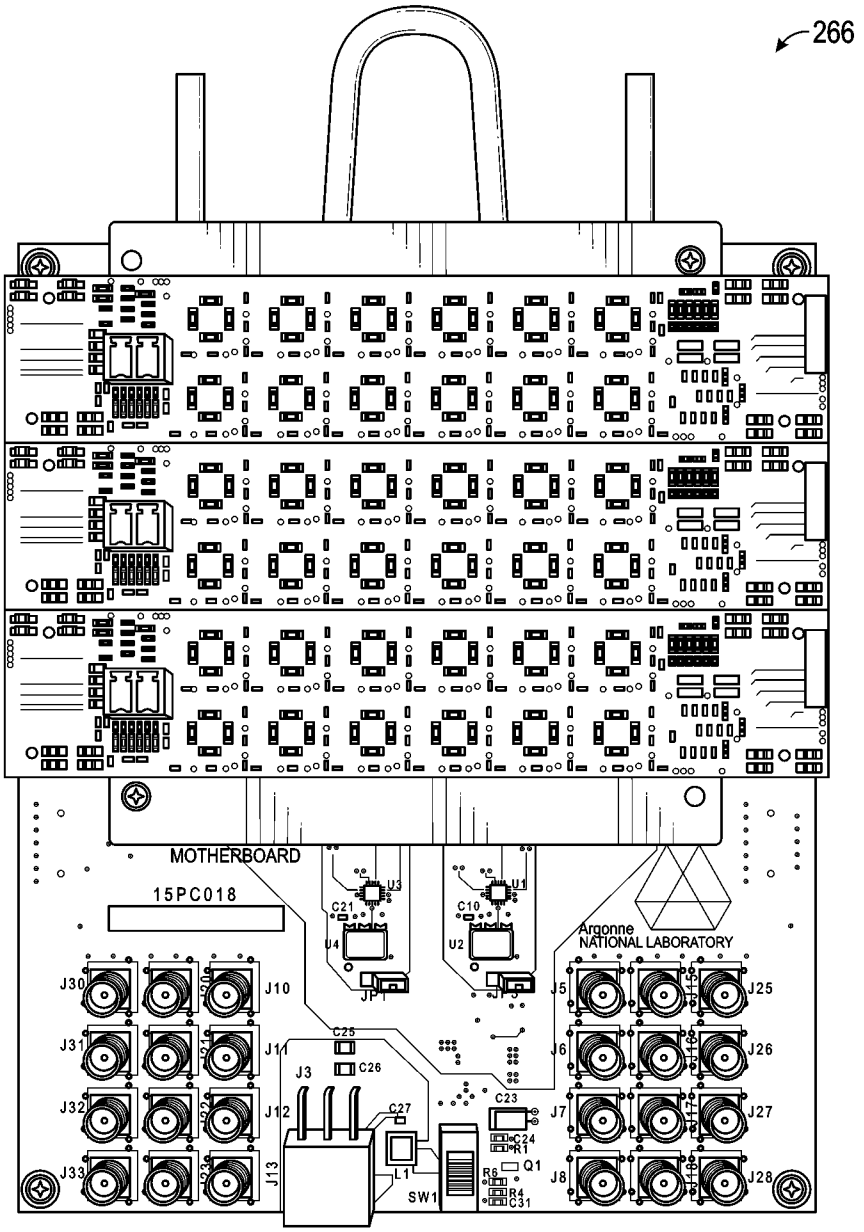

266
MOTHERBOARD
15PC018
Argonne
NATIONAL LABORATORY
J30
J31
J32
J33
J10
J11
J12
J13
J3
J5
J6
J7
J8
J25
J26
J27
J28
U1
U2
U3
U4
C10
C21
C23
C24
C25
C26
C27
R1
R4
R6
C31
Q1
L1
SW1
JP1

FIG. 22

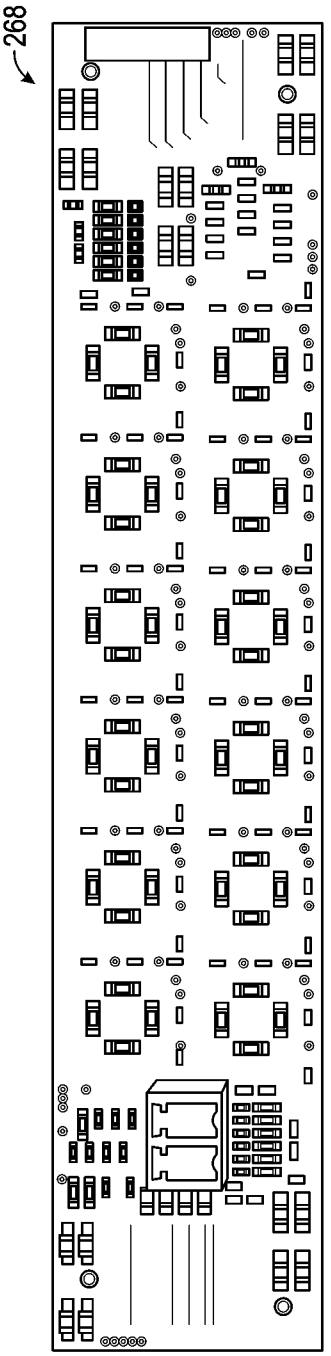


FIG. 23

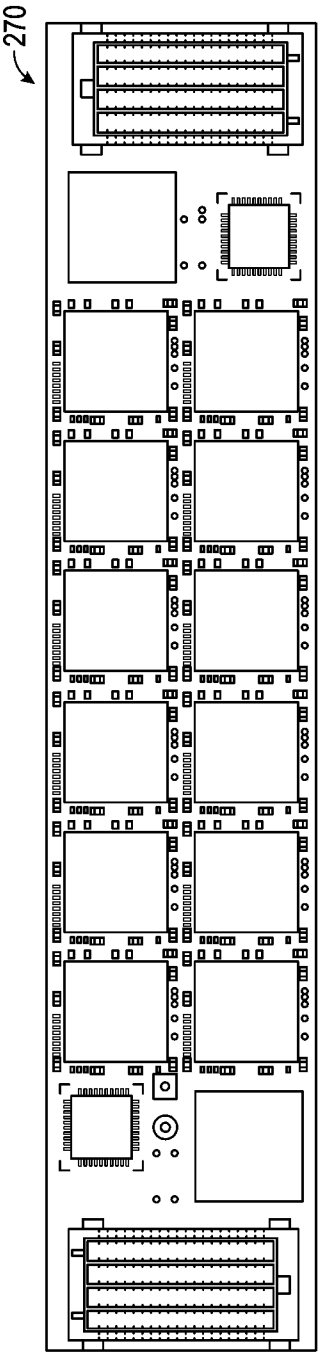


FIG. 24

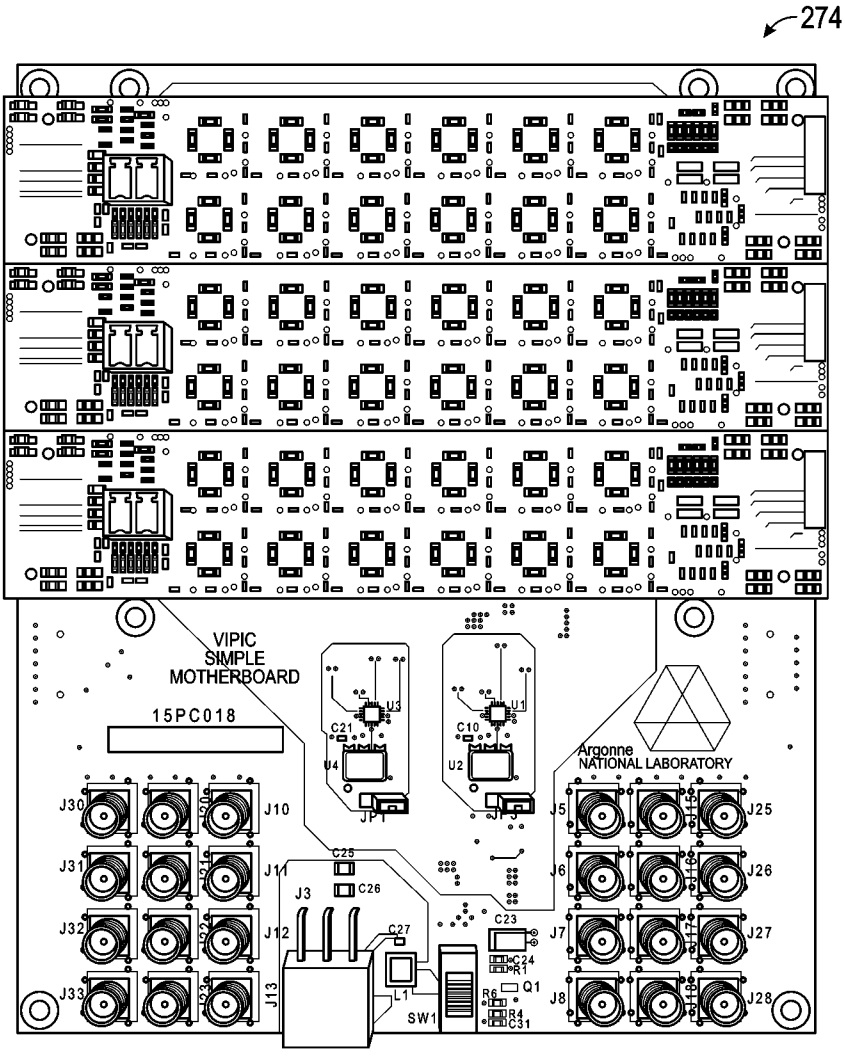

274
VIPIC
SIMPLE
MOTHERBOARD
15PC018
Argonne
NATIONAL LABORATORY
J30
J31
J32
J33
J10
J11
J12
J13
J3
J5
J6
J7
J8
J25
J26
J27
J28
U1
U2
U3
U4
C10
C21
C23
C24
C25
C26
C27
C31
R1
R4
R6
Q1
L1
SW1
JP1
JP3

FIG. 25

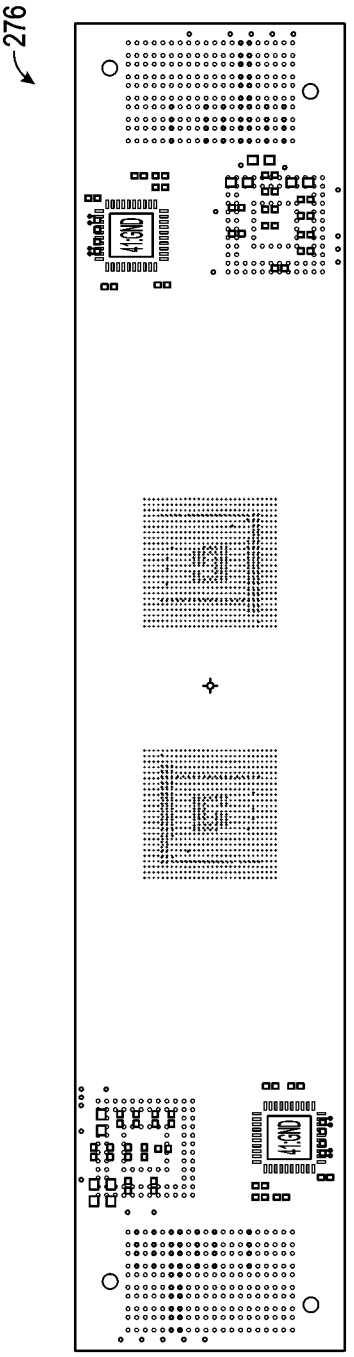


FIG. 26

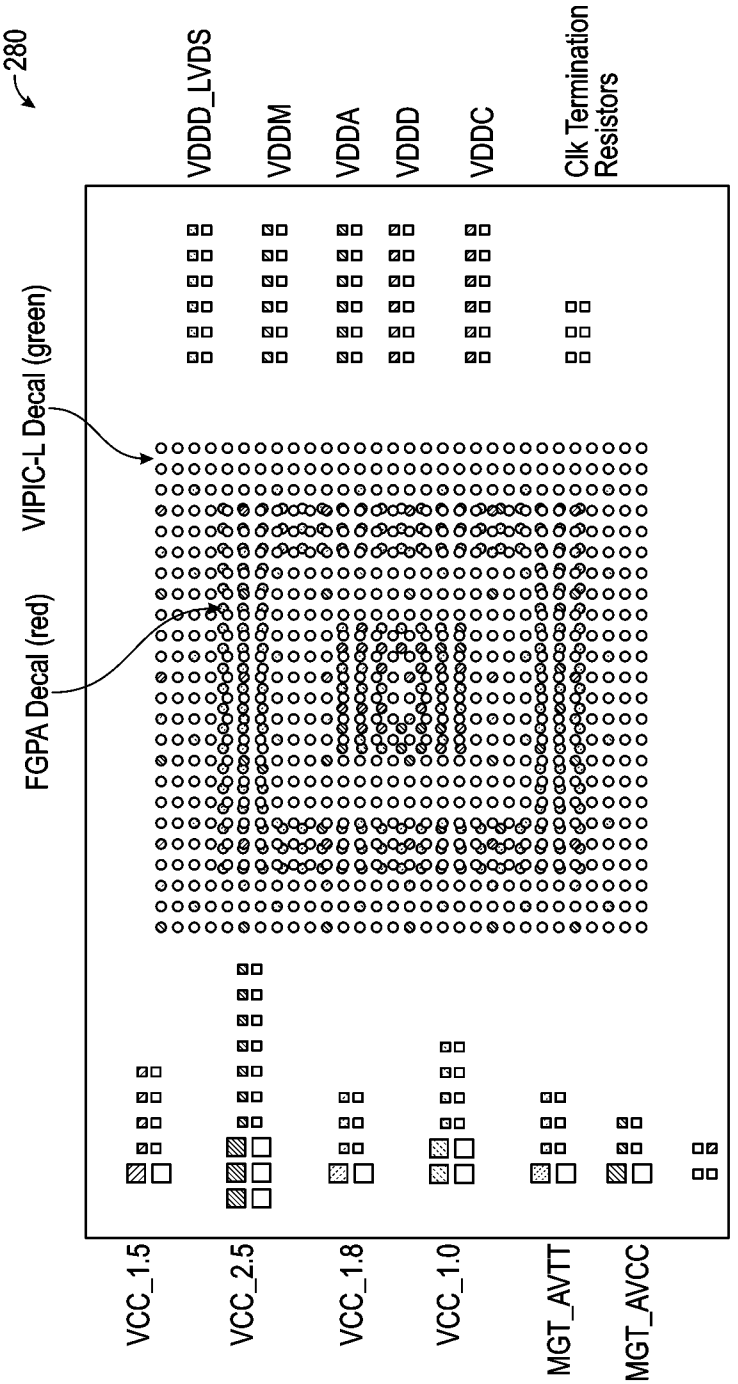

280
VDD_LVDS
VDDM
VDDA
VDDD
VDDC
Clk Termination Resistors
VIPIC-L Decal (green)
FGPA Decal (red)
VCC_1.5
VCC_2.5
VCC_1.8
VCC_1.0
MGT_AVTT
MGT_AVCC

FIG. 27

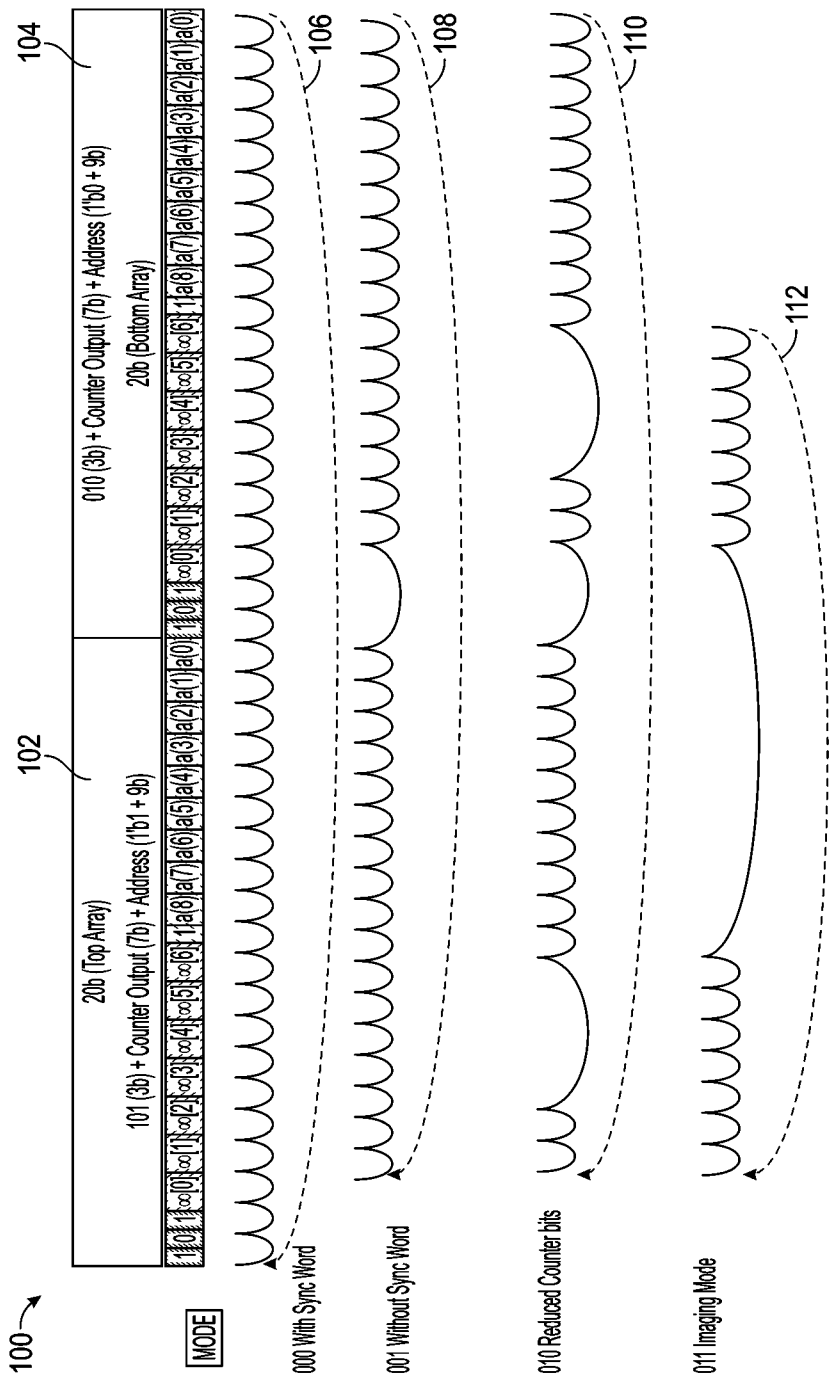

100
102
104
20b (Top Array)
101 (3b) + Counter Output (7b) + Address (1'b1 + 9b)
010 (3b) + Counter Output (7b) + Address (1'b0 + 9b)
20b (Bottom Array)
MODE
000 With Sync Word
001 Without Sync Word
010 Reduced Counter bits
011 Imaging Mode
106
108
110
112

FIG. 28

EDGELESS LARGE AREA CAMERA SYSTEM

CROSS-REFERENCE TO PROVISIONAL APPLICATION

[0001] This patent application claims priority under 35 U.S.C. 119(e) to U.S. Provisional Patent Application Ser. No. 62/195,053 entitled "VERTICALLY INTEGRATED PHOTON IMAGING CHIP DETECTOR FOR X-RAY SPECTROSCOPY," which was filed on Jul. 21, 2015, the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] Embodiments are generally related to a camera. Embodiments are also related to ceramic board or PCB with 3D (three dimensional) ASIC (Application Specific Integrated Circuit), wafer scale-large area sensor, FPGA (Field Programmable Gate Arrays), with cooling systems, data acquisition systems and other circuit components and devices. Embodiments further relate to an apparatus for an edgeless large area camera utilized in detection applications and methods of configuring such an apparatus. Embodiments further relate to a VIPIC (Vertically Integrated Photon Imaging Chip) camera.

BACKGROUND

[0003] Camera system's specifically optimized for X-ray Photon Correlation Spectroscopy (XPCS) involve imaging "speckle" patterns produced when a coherent beam of x-rays scatters off a disordered sample. The speckle pattern is essentially the superposition of many single-particle diffraction patterns produced by the atoms within the sample. As the atoms undergo motion, the speckle pattern changes, so XPCS can be used to study atomic dynamics at very short time and distance scales. Use of XPCS will continue to expand for applications associated with x-ray light sources in coming years, particularly as synchrotrons upgrade to increase coherence.

[0004] Speckle patterns produce an anomalously weak signal With average pixel occupancies <<1%, XPCS is not well suited to a traditional x-ray area detectors which read out every pixel on every exposure. Much of the data throughput would be spent processing empty pixels.

BRIEF SUMMARY

[0005] The following summary is provided to facilitate an understanding of some of the innovative features unique to the disclosed embodiments and is not intended to be a full description. A full appreciation of the various aspects of the embodiments disclosed herein can be gained by taking the entire specification claims, drawings, and abstract as a whole.

[0006] It is, therefore, one aspect of the disclosed embodiments to provide for a 3D Integrated camera system.

[0007] It is another aspect of the disclosed embodiments to provide for a large area camera with a large area sensor 3D bonded to an array of 3D integrated ASICs which is further connected to a PCB or ceramic board on one side and an array of FPGA's on the other side constituting a detector module. An array of detector modules can be then connected to a detector head which also includes a cooling system in close proximity to allow for thermal management of the system and a plurality of picozed modules to connect to a data acquisition system.

[0008] It is another aspect of the disclosed embodiments to provide for improved ASIC (Application Specific Integrates Circuit) functionality, components and devices.

[0009] It yet another aspect of the disclosed embodiments to provide an edgeless large area ASIC utilized in detection applications.

[0010] It still another aspect of the disclosed embodiments to provide a ceramic substrate upon which one or more ASIC layers of a multi-tier ASIC layer is electrically connected (e.g., bump bonded). Such a ceramic substrate can be, for example, a low thermal co-fired ceramic.

[0011] It is also an aspect of the disclosed embodiments to configure the aforementioned ceramic substrate (e.g., on the other side) with one or more FPGAs electrically connected (e.g., bump bonded) to constitute a detector module.

[0012] In yet another aspect of the disclosed embodiments, the detector head can behave as a data concentrator composed of several detector modules and other circuit components to transfer high speed data to a DAS (data acquisition system) capable of implementing real-time correlation algorithms.

[0013] It is another aspect of the disclosed embodiments to provide for an edgeless large are camera system.

[0014] The aforementioned aspects and other objectives and advantages can now be achieved as described herein. In an example embodiment, a three dimensional integrated edgeless pixel detector apparatus can be implemented, which includes a large area three tier three-dimensional detector having one sensor layer, and two ASIC layers comprising an analog tier and a digital tier configured for x-ray photon counting and time of arrival measurement and imaging. The camera system consisting of a detector head with a cooling system, connectors for data transfer to an external data acquisition system and several detector modules each containing several FPGAs and 3D integrated ASICs and sensor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying figures, in which like reference numerals refer to identical or functionally-similar elements throughout the separate views and which are incorporated in and form a part of the specification, further illustrate the present invention and, together with the detailed description of the invention, serve to explain the principles of the present invention.

[0016] FIG. **1** illustrates a side cut-away view of a single module 3D integrated edge detector apparatus, in accordance with an example embodiment;

[0017] FIG. **2** illustrates a diagram depicting the layout of a VIPIC-L Analog Chip, in accordance with an example embodiment;

[0018] FIG. **3** illustrates a diagram depicting the layout of a VIPIC-L Digital Chip, in accordance with an example embodiment;

[0019] FIG. **4** illustrates a diagram depicting the back of a VIPIC-L digital chip with names of the bump-bond I/O connections which need to be connected to the PCB or ceramic board in accordance with an example embodiment;

[0020] FIG. **5** illustrates an analog pixel bonding interface layout with locations of the various analog functional block

layouts connecting to the analog pixel on one side and a part of the digital sub-chip on the other, in accordance with an example embodiment;

[0021] FIGS. **6-7** illustrate respective sub-chip layouts having the sub-chip digital functionality shown in FIG. **14**, in accordance with an example embodiment;

[0022] FIG. **8** illustrates a flow chart of operations depicting logical operational steps of a method for configuring an edgeless large area ASIC in accordance with an example embodiment;

[0023] FIG. **9** illustrates layout diagrams of a VIPIC digital tier and a VIPIC analog tier having washable analog test PADS with connections in the analog tier, (Please note that these pads are not shown to scale, they fit in the 5 um boundary of a 1.25 cm×1.25 cm ASIC), in accordance with an example embodiment;

[0024] FIG. **10** illustrates a schematic diagram depicting an analog pixel circuit, which can be implemented in accordance with an example embodiment;

[0025] FIG. **11** illustrates a schematic diagram depicting a charge amplifier circuit, which can be implemented in accordance with an example embodiment;

[0026] FIG. **12** illustrates a schematic diagram depicting a test injection circuit, which can be implemented in accordance with an example embodiment;

[0027] FIG. **13** illustrates a diagram of an analog pixel layout, in accordance with an example embodiment;

[0028] FIG. **14** illustrates a block diagram of a digital sub-chip, in accordance with an example embodiment;

[0029] FIG. **15** illustrates a schematic diagram of a first part of the detector system in accordance with an example embodiment;

[0030] FIG. **16** illustrates a schematic diagram of a second part of the detector system, which can be implemented in accordance with another example embodiment;

[0031] FIG. **17** illustrates a VIPIC motherboard with three detector modules installed and a PicoZed module, which can be implemented in accordance with an example embodiment;

[0032] FIG. **18** illustrates top and side views of a detector module, in accordance with an example embodiment;

[0033] FIG. **19** illustrates an image of a VIPIC motherboard (view of the PicoZed Side), in accordance with an example embodiment;

[0034] FIG. **20** illustrates an image of the VIPIC motherboard shown in FIG. **19** with a view from the detector module side, with one detector module plugged in, in accordance with an example embodiment;

[0035] FIG. **21** illustrates a VIPIC motherboard PCB layout, in accordance with an example embodiment;

[0036] FIG. **22** illustrates an image of three VIPIC detector modules (FPGA only) on a simple VIPIC motherboard with a water cooling plate, in accordance with an example embodiment;

[0037] FIGS. **23-24** illustrate top and bottom of a FPGA only detector module, which can be implemented in accordance with an example embodiment (Note: FIG. **23** depicts thermal resistors instead of VIPIC ASICs for thermal dissipation studies);

[0038] FIG. **25** illustrates an image of three VIPIC detector modules (FPGA only) on a simple VIPIC motherboard before mounting the cooling system, in accordance with an example embodiment;

[0039] FIG. **26** illustrates a VIPIC detector module with connection pattern to two 3D ASICs, in accordance with an example embodiment.

[0040] FIG. **27** illustrates a ball grid array pattern for an FPGA and an ASIC along with all the power supplies required for both, while demonstrating the complexity required for routing and the lack of space for mounting additional components, in accordance with an example embodiment; and

[0041] FIG. **28** illustrates examples of configurable readout modes, can change bit stream patterns, in accordance with an example embodiment.

DETAILED DESCRIPTION

[0042] The particular values and configurations discussed in these non-limiting examples can be varied and are cited merely to illustrate one or more embodiments and are not intended to limit the scope thereof.

[0043] Subject matter will now be described more fully hereinafter with reference to the accompanying drawings, which form a part hereof, and which show, by way of illustration, specific example embodiments. Subject matter may, however, be embodied in a variety of different forms and, therefore, covered or claimed subject matter is intended to be construed as not being limited to any example embodiments set forth herein; example embodiments are provided merely to be illustrative. Likewise, a reasonably broad scope for claimed or covered subject matter is intended. Among other things, for example, subject matter may be embodied as methods, devices, components, or systems.

[0044] Throughout the specification and claims, terms may have nuanced meanings suggested or implied in context beyond an explicitly stated meaning. Likewise, the phrase "in one embodiment" or "in one example embodiment" as used herein does not necessarily refer to the same embodiment and the phrase In another embodiment" or "in another example embodiments" as used herein does not necessarily refer to a different embodiment. It is intended, for example, that claimed subject matter include combinations of example embodiments in whole or in part.

[0045] In general, terminology may be understood, at least in part, from usage in context. For example, terms, such as "and," "or," or "and/or" as used herein may include a variety of meanings that may depend, at least in part, upon the context in which such terms are used. Typically, "or" if used to associate a list, such as A, B, or C, is intended to mean A, B, and C, here used in the inclusive sense, as well as A, B, or C, here used in the exclusive sense. In addition, the terms "at least one" or "one or more" as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures, or characteristics in a plural sense. Similarly, terms such as "a," "an," or "the," again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term "based on" may be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0046] As discussed previously, a detector specifically optimized for X-ray Photon Correlation Spectroscopy (XPCS) involves imaging "speckle" patterns produced when a coherent beam of x-rays scatters off a disordered sample.

The speckle pattern is essentially the superposition of many single-particle diffraction patterns produced by the atoms within the sample. As the atoms undergo motion, the speckle pattern changes, so XPCS can be used to study atomic dynamics at very short time and distance scales. Use of XPCS will continue to expand for applications associated with x-ray light sources in coming years, particularly as synchrotrons upgrade to increase coherence.

[0047] Speckle patterns can produce an anomalously weak signal. With average pixel occupancies <<1%, XPCS is not well suited to a traditional x-ray area detectors which read out every pixel on every exposure. Much of the data throughput would be spent processing empty pixels.

[0048] A technique-specific detector utilizing a Vertically Integrated Photon Imaging Chip (VIPIC) can provide several unique capabilities designed to address the challenges of XPCS and enable new science. These properties include sparsified readout, high time resolution, and real-time calculation of auto-correlation functions.

[0049] Regarding sparsified readout, the VIPIC detector will increase data throughput by only reading out those pixels receiving an x-ray hit during the exposure window. The basic raw data is a simple list of hit times and pixel locations. The detector dispenses with the standard notion of an exposure producing a new imaging regime optimized for low-signal techniques.

[0050] Regarding high-time resolution, the detector can specify the interaction time of an x-ray to better than, for example, 10 microseconds. Standard area detectors simply record the location of the interaction, and the temporal resolution is determined by the exposure time.

[0051] Regarding real-time calculation of auto-correlation functions, the final result of an XPCS measurement is an auto-correlation function. The VIPIC detector will include novel readout electronics capable of real-time calculation of the auto-correlation functions. A practical detector for this purpose demands a large pixel count in order to acquire sufficient events to give good statistics.

[0052] The disclosed example embodiments discussed and illustrated herein cover various aspects of a very new technology of 3D integration that allows for an enhanced functionality in a hybrid pixel detector (e.g., a low noise, sparsified readout with a time stamp providing less than 10 microseconds precision). 3D integration comprises a method in which two separate CMOS circuits are bonded together, mechanically and electrically, to provide greater functionality than would be possible in a single CMOS layer. VIPIC utilizes a two-layer ASIC which will be directly bonded to a pixilated silicon sensor, and the resulting sensor/ASIC hybrids will be bump-bonded to a ceramic readout board. The unique hybrid structure does not require traditional wire-bonds for readout of the ASICs, eliminating many of the coverage gaps associated with traditional hybrid pixel area detectors.

[0053] Note that a TSV (through-silicon via) is a vertical electrical connection (via) passing completely through a silicon wafer or die. TSVs can be utilized to create 3D packages and 3D integrated circuits, compared to alternatives such as package-on-package because the density of the vias is substantially higher, and because the length of the connections is shorter.

[0054] FIG. **1** illustrates a side cut-away view of a single module 3D integrated edge detector apparatus **10**, in accordance with an example embodiment. The apparatus **10** depicted in FIG. **1** can function as a 3D integrated edgeless pixel detectors and generally includes a cooling plate **12** disposed adjacent to a group FPGA (Field-Programmable Gate Array) devices **14**, **16**, **18**, **20** configured on an LTCC (Low Thermal Coefficient Ceramic) substrate **24** in association with a connector chip **22** which in turn is electrically connected to a lead wire **23** for connection to other electrical devices and components. A group of ASIC devices **34**, **36**, **38**, **40** is located below the LTCC substrate **24** at positions corresponding approximately to the locations of the respective FPGA devices **14**, **16**, **18**, **20**. The ASIC devices **34**, **36**, **38**, **40** can form an ASIC array, and the FPGA devices **14**, **16**, **18**, **20** can form an FPGA array. The ASIC devices **34**, **36**, **38**, **40** are located on an oxide layer **28** that in turn is located above an HR sensor slab/wafer **30**. The ASIC devices **34**, **36**, **38**, **40** can form part of a 3D ASIC device.

[0055] A large area **3**-tier 3D detector with one sensor layer, such as the sensor layer **30**, and two ASIC layers containing one analog and one digital tier can be configured for x-ray photon counting and time of arrival measurement and imaging.

[0056] In some example embodiments, a full custom analog pixel shown in FIG. **13** can be, for example, 65 μm×65 μm. Such an analog pixel can be connected to a sensor pixel of the same size on one side, and on the other side can offer approximately 40 connections to the virtual digital pixel.

[0057] The analog tier can be configured with no peripheral functional blocks. Hence, the active area extends to the edge of the detector. This arrangement can be achieved by utilizing a few flavors of almost identical analog pixels (e.g., with minimal variation in layout) to allow for peripheral biasing blocks to be placed within pixels.

[0058] In one embodiment, on the sensor tier, a large array of for example, 385×1157 array of for example, 65 μm×65 μm, will be connected to for example 12, 3D integrated ASICs, with sub-pixel or at most one pixel minimum gap between each ASIC. The 1 row and 5 columns of unconnected (to ASIC) pixels are connected to ground or left floating.

[0059] In another embodiment, on the sensor tier, a large array of for example, 384×1152 array of pixels will be connected to for example 12, 3D integrated ASICs, with a minimum gap of 65 μm between each ASIC. Such that 2 row and 10 columns of pixels located in between ASIC's are elongated to 1.5 times the size of the pixel to create a dead-zone less sensor system.

[0060] On the Analog ASIC tier, a 192×192 edgeless array has no peripheral functional blocks, for example. The pixels are arranged to create an entire 1.248 cm×1.248 cm ASIC as shown in FIG. **2**. A small area within a 64×32 pixels is reserved for getting Analog I/O through the Digital tier from the PCB or other ceramic board. This I/O connectivity layout is repeated in a 3×6 array to provide connectivity for the entire ASIC.

[0061] On the Digital ASIC tier, a 32×32 edgeless array without any peripheral functional blocks, for example, constitutes a sub-chip. Such an example sub-chip can be an indivisible unit, which is further arranged in, for example, a 6×6 array to create an entire 1.248 cm×1.248 cm ASIC as shown in FIG. **3**.

[0062] Each chip can include **720** bump-bond I/O connections shown in FIG. **4** on the back of the digital tier to the ceramic PCB or substrate such as, for example, the LTCC substrate **34** shown in FIG. **1**. The entire analog tier power

and biasing can be conveyed through the digital tier from the PCB or ceramic substrate **24**.

[0063] FIG. **5** illustrates the analog pixel bonding interface layout with locations of the various analog functional block layouts connecting to the analog pixel on one side and a part of the digital sub-chip on the other. Approximately 25% of the bonding interface contains electrical connections between the analog and digital tier, these connections have a zip via between the zip plug and metal 8. The rest of the connections provide mechanical bonding and do not contain zip via.

[0064] FIGS. **6** and **7** illustrate the sub-chip layout (**82** and **84**) with sub-chip digital functionality shown in FIG. **14**, in accordance with an example embodiment. Each sub-chip can contain, for example, 20 bump-bond pads for external **110**'s, they are created using back metal connected to Metal 1 in the ASIC via multiple B-TSVs (through-silicon vias) (preferably more than 100 per group). These bump-bond pads can, for example, 60 μm×60 μm in size, and can be placed with a horizontal and vertical pitch of, for example, 520 μm and 416 μm respectively. Routing of higher density bump-bond pads on the readout board would require very aggressive sizes and separation of traces. A total of, for example, 720 bump-bond pads can be utilized per VIPIC.

[0065] To minimize complexity, global signals can be shared between two sub-chips as shown in FIGS. **6** and **7**. The 14 analog power and bias signals can be distributed on the top and bottom of the sub-chip, these need to be connected from Metal 1 to 9 on the digital tier, which is then electrically connected to Metal 9 of the Analog tier and subsequently distributed to the analog pixel. Shared signals can also include digital signals used for analog calibration, StrobeN and StrobeP, digital reset and frameClk. Configuration register clock and I/O and serializer differential I/O (e.g., see the output serializer **68** shown in FIG. **14**) can be dedicated signals for a sub-chip.

[0066] The bump-bond pad sizes are approximately the same size as a pixel. The analog bump-bond pads, irrespective of their placement within a sub-chip, will partially overlap with inter-pixel electrical connectivity at fixed locations every, for example, 65 μm. Hence, these need to be custom designed to make sure that the inter-pixel connections are not shorted to global signals.

[0067] These bump-bond pads also create routing and placement restrictions in certain areas across the digital sub-chip. A power and ground grid for digital VDD and VSS can be created utilizing top two metal layers (e.g., vertical Metal 8 and horizontal Metal 7) approximately 10 μm wide at 65 μm pitch.

[0068] An embodiment of the Analog pixel architecture is shown in FIG. **10**, which contains a charge sensitive amplifier with leakage current compensation followed by a shaping amplifier, AC-coupled to the first stage of two comparator pre-amplifiers, and two additional comparators. Each comparator pre-amplifiers also receive inputs from trimming digital to analog converters (DAC) for offset correction.

[0069] In an example embodiment, the window discriminator can contain two comparators with an upper and lower threshold to enable energy discrimination. Energy spectroscopy can be performed by increasing the number of comparators with additional thresholds within a pixel or using an in-pixel analog to digital converter (ADC).

[0070] A preamplifier circuit is shown in FIG. **11**; its feedback network contains a leakage current compensation circuit. It also contains additional capacitors in the feedback for gain trimming.

[0071] A test injection circuit contained in each pixel is shown in FIG. **12**, which is used for calibrating the pixel.

[0072] The hit processor, accepts the output of the window discriminator from the analog tier and increments a, for example, a 7-bit gray-counter to register the number of photon hits in the pixel in a given time frame (frameClk). Since the pixel has two 7-bit counters for dead-time less operation, at any given time, one counter is in 'count mode' and the other is in 'read mode' if it had valid data in the previous frame or is 'idle'. At the rising edge of the frameClk, the counters which were in 'read mode' hut not yet read out will be reset, while those in 'count mode' with valid data will be swapped and placed in 'read mode'.

[0073] Counters, which were not used, can remain in the "count mode." This feature conserves power in low occupancy detector applications. The logic that checks if the counter is occupied and asynchronously resets it after readout, is extremely sensitive to glitches. Hence, a gray-code counter is preferable to a binary ripple counter to reduce the number of switching bits. Additionally, the choice of a gray-code counter reduces power consumption. Spill over protection logic eliminates the data recorded in the previous frame to be allocated to the wrong frame if the entire array was not fully read. Several user-defined functions can also be added such as utilizing only a single comparator instead of a window discriminator etc. The design is asynchronous, without the requirement of a high-speed clock tree distribution, as the data is generated by photon arrival. Full analog simulations were performed which clearly indicated that the design is sensitive to parasitics and a full custom layout, as disclosed herein, is required. 1024 hit processor full custom layout blocks can be strategically located across the sub-chip, close to the comparator outputs from the analog tier.

[0074] The priority encoder (e.g., see the priority encoder (top) and priority encoder (bottom) shown in FIG. **14**) can be utilized for zero-suppression of data. This also increases the data throughput by only reading those pixels, which received photon hits during the time frame (exposure window) defined by the frameClk. The basic data is a simple list of counter value and pixel location. The priority encoder is a binary tree and also generates the address of the pixel. The priority encoder can be divided into two parts each generating a 9-bit address for 512 pixels. This allows access of the two parts in an interleaved manner, providing enough time for the address bus to settle when a pixel is selected.

[0075] FIG. **14** illustrates a schematic diagram depicting a readout from the output serializer **68** with respect to different modes of operation, in accordance with an example embodiment. The example different modes of operation depicted in FIG. **28** are modes **106**, **108**, **110**, **112**. Mode **108** involves "000 with sync word." Mode **108** involves "001 without sync word. " Mode **110** involves "010 reduced counter bits" and mode **112** is a "011 imaging mode".

[0076] Regarding managing data transfer, photons arriving asynchronously at the detector generate a charge in the sensor, which can be processed by the analog pixel and subsequently events can be counted in the digital pixel within a certain time period. This time period can be determined externally by the user and defined within the ASIC as one period of the frameClk. The resolution of

measure of photon time of arrival information can be determined by frameClk, which can typically range from a few hundred nanoseconds to a few tens of microseconds depending on the application. Typically, it is set at <10 μs. The change of frame caused by the rising edge of the frameClk creates a new priority list for pixel readout established by the priority encoder.

[0077] For certain applications, the frameClk rates need to be considerably faster than ~200 ns. However only 4 valid data packets at a data transfer rate of 50 ns/data packet can be read within this time frame. A really short exposure time, results in very few events. Hence a 7-bit counter will certainly not be fully occupied. Thus truncating the counter to, for example, 2-bits will be sufficient. Hence various readout modes are developed, to change the length of the data packet, which reduce the time for data transfer/packet.

[0078] The high-speed output serializerClk is independent of the slower ~1 μs frameClk, which are generally not aligned with each other. Although synchronizing the two clocks is possible, the application might require an independent setup of the frameClk and serializerClk. Furthermore, synchronization still does not guarantee correct alignment of the two signals at the pixel, because the clock tree for the frameClk is different from the path readoutControl (derived from the serializerClk) utilized through the priority encoder. The delays of these signals are position dependent and cannot be well controlled for a high-speed system. The power penalty from buffering and managing the clock tree of a slow clock with a high-speed clock is unnecessary, and practically unfeasible. However, it is important to ensure that data integrity is maintained during frame changes. A novel technique for ensuring that high priority data is not corrupted during frame changes can be implemented.

[0079] The full output data packet can include, for example, a 3-bit synchronization header, a 7-bit counter value and a 10 bit pixel address. This data can be serially transferred using high-speed differential outputs and an output serializerClk running at, for example, ~400 MHz.

[0080] Regarding readout modes, the data output of the ASIC can be either operated in a zero-suppressed or full-frame imaging format, which results in different data packet lengths. In the zero-suppressed format, the data packet needs to contain the 10-bit pixel address and between 2-7 bits of counter value, furthermore the 3-bit synchronization header is optional (but may be essential for debugging). In this case, for example a 20-bit data packet transfers a 3-bit start symbol, a 10-bit pixel address and a 7-bit counter value, requiring 50 ns to transfer a single data packet, or a 10-bit pixel address and 2-bit counter value, requires 30 ns. In the full imaging format, since every pixel is read out, only the 7-bit counter value is required, with 17.5 ns for readout per data packet, which achieves a 55 kfps for a 1Mpixel detector. This may increase considerably if fewer counter bits are chosen.

[0081] FIG. **28** thus shows the main readout modes **106** **108**, **110** and **112** discussed previously.

[0082] Maintaining data integrity at frame changes presents a challenge. During the current time frame, each pixel with valid data, sends a request signal for read out, to the priority encoder. The priority encoder (e.g., priority encoder (top) **70** and priority encode (bottom) **76**) establishes the order in which the pixels are allowed to transfer data to the output serializer **68**. The output serializer **68** allows a specific time window for the counter output to be transferred and the address to become available, such that it can be latched in time for off-chip data transfer (by the loadSerializer).

[0083] The rising edge of the frameClk, changes the frame. Counters in the 'readout mode' are reset, those in the 'count mode' are changed to 'readout mode' and those that are 'idle' do not change. Simultaneously, the priority encoder creates a new priority list by assigning the order in which multiple pixels are read out. The following signals are involved in data readout: frameClk, readoutControl, selectPixel (n), and load serializer.

[0084] The signal frameClk is a rising edge used to indicate change of frame (external slow clock). The signal readoutControl can be used to enable data transfer from a pixel to the serializer register, which is generated by the output serializer. This signal is interleaved between the two 512 pixel banks and is alternately broadcasted to the top pixel matrix and then to the bottom pixel matrix for pixel selection. The readoutControl pulse width is 2.5 ns corresponding to the serializerClk of 400 MHz. The time between the pulses of readoutControl is set by the readout mode depending on the number of output bits.

[0085] The rising edge of the frameClk, triggers the rising edge of readoutControl for both the top and bottom halves. This disables the last pixel being readout before the frame changes. The readoutControl is then held high up until at least one complete readout cycle is finished. The frameClk, distributed to the pixels is then delayed to the middle of the high state created on the readoutControl. This ensures the arrival of frameClk edge to any pixel in the matrix when readoutControl is high. Adjusting these signals in this manner leads to a minimal unavoidable dead-time in the readout of data. The following sequence with a time frame change is achieved on the output serial link: two unavoidably corrupted last data outputs, two known data patterns corresponding to frame change and then restarting readout with data from the top of the priority list in the new frame.

[0086] As discussed herein, in some examples, several readout modes can be implemented to allow the user to redefine a data packet and change the output data rate. It can therefore be appreciated that a novel technique and apparatus can thus be implemented, as disclosed herein, which can ensure that high priority data is not corrupted during frame changes.

[0087] FIG. **16** illustrates a flow chart of operations depicting logical operational steps of a method **700** for configuring an edgeless large area ASIC in accordance with an example embodiment. As shown at block **705**, the process can be initiated. Then, as indicated at block **710**, an operation can be implemented to post process foundry ASIC wafers. Next, as illustrated at block **715**, a step or operation can be implemented to add an extra metal layer to create metal bonding posts. Then, as shown at block **720**, a step or operation can be implemented to face-to-face fusion bond analog and digital ASIC tiers at the wafer-to-wafer level. Next, as depicted at block **725**, a step or operation can be implemented to thin and planarize one side of the arrangement. Thereafter, as indicated at block **730**, a step or operation can be implemented to insert TSVs (through-silicon vias).

[0088] Following processing of the operation depicted at block **735**, a step or operation can be provided to pattern back metal. Then, as shown at block **740**, a step or operation can be implemented to deposit a new layer of oxide and

bond to the silicon handle wafer. Thereafter, as shown at block **745**, a step or operation can be provided to repeat thinning, planarizing and patterning steps/operations.

[0089] Temporary washable PADs as shown in FIG. **27** are added to test known good dies. Please note FIG. **27** is not to scale the temporary washable pads are in the 5 um periphery and the ASIC is approximately 1.25 cm×1.25 cm

[0090] A map of known good dies is identified by testing the configuration register on the digital side and the analog biases on the analog side.

[0091] Thereafter, as shown at block **750**, a step or operation can be implemented to dice the wafer and implement a die-to-wafer fusion bond array of KDG (known good die) to sensor wafer. Then, as illustrated at block **755**, a step or operation can be implemented to remove the handle wafer to expose the backside pads on the digital tier. The process can then end, as indicated at block **760**.

[0092] FIG. **15** illustrates a diagram of the entire system. The VIPIC Detector System shown in FIG. **15** is composed of a detector head, a cooling system, a power supply, a user interface computer and a data acquisition system.

[0093] The detector head as shown in FIG. **16** is composed of a VIPIC mother board, populated with three detector modules and a commercial PicoZED board.

[0094] The VIPIC mother board as shown in FIG. **17** provides a number of features such as, for example, the ability to hold the PicoZED module with Zynq FPGA running Linux. The configuration depicted in FIG. **17** can also hold three VIPIC detector modules. In addition, VIPIC mother board depicted in FIG. **17** can provide system clocks to Artix chips and VIPIC ASICs, and also provide, for example, a 1 Gbit Ethernet Connection for slow controls, and a 10 Gbit Ethernet connection for faster communications. The FIG. **17** arrangement can also provide for an SD card for PicoZED Linux and FPGA, and can also include 6 miniPODs, which have 12 fibers each and are used to communicate to the Artix FPGAs and through them transmit the VIPIC ASIC data.

[0095] The system shown in FIG. **17** also allows the PicoZED to monitor and control two transmit and receive ports coming from two Artix chips and going to the miniPODs. Such a system can also include 22 voltage regulators to power PicoZED, Artix FPGAs. Additionally, the VIPIC ASICs can include a USB part for a Linux console and JTAG interfaces to Artix and PicoZED. Trigger inputs and outputs are also provided with respect to the FIG. **17** configuration.

[0096] The top and bottom view of a partially assembled mother board are depicted in FIGS. **19** and **20**, while a detailed layout of one of its layers is shown in FIG. **21**.

[0097] Note that PicoZED module is a commercial board that simplifies the software and hardware development needed to communicate and control the detector head. The PicoZED module offers a Xilinx Zynq FPGA running Linux on its dual ARM processors. Thus, the PicoZED module allows for development in a Linux environment similar to that of, for example, a Linux computer. In addition to the ARM processors, the Xilinx Zynq has a reprogrammable FPGA section, allowing for the development of custom logic to perform task that cannot be handled by the Linux software.

[0098] FIG. **18** illustrates the assembly of a detector module on an electrical substrate (PCB or ceramic board such as LTCC). In an example embodiment a detector module can include an array of 2×6 3D integrated VIPIC's connected on one side to the sensor and bump bonded on the opposite side to the PCB. Further as shown in FIG. **24**, the opposite side of the PCB can be bonded to an array of 2×6 FPGA's. This configuration also contains connectors on the edges, which allow signal transfer from a detector module to the detector head.

[0099] The detector module has almost 12,000 solder bumps in an area of 25 mm×75 mm, which requires high density ball grid array packaging on both top and bottom of the printed circuit board as well as surface mount components in 01005 case sizes. The layout, routing and fabrication of this board will require state of the art techniques utilizing 24+ layers as well as via-in-pad, stacked laser drilled microvias and multiple lamination cycles.

[0100] With 12 ASICs on each detector module, each having hundreds of I/O, it was critical to minimize this interconnect as close to the front end as possible, therefore the design matches each ASIC with its own FPGA. The FPGA then consolidates all the complexities of the ASIC interconnect into a single high speed bidirectional 5 Gbps link for communication with the data acquisition system.

[0101] The Detector Module has 12 Artix FPGAs and 12 VIPIC ASICs. It is designed so that there is one Artix FPGA for each VIPIC ASIC. The Artix FPGA and VIPIC ASIC are placed on opposite sides of a PCB board making it necessary for the PCB to use buried vias in order to route the traces between the BGA (ball grid array) parts. Each Artix FPGA collects the data from its associated VIPIC ASIC over its 36 LVDS outputs from. Inside the Artix FPGA, all of this data is then concentrated into a single multi-gigabit transmitter. This transmitter can be routed through the VIPIC detector head to a miniPOD transmit fiber. In this manner, the data from each VIPIC ASIC can be concentrated into a single fiber output.

[0102] The cooling system can be composed of a chiller and a heat exchanger. The heat exchange is within the detector head and located between the VIPIC mother board and the three Detector Modules

[0103] The Power Supply can provide power to the detector head. The power goes into the VIPIC mother board which generates all of the various voltages need by the PicoZED board and the detector module. The voltages needed by the detector module are for the Artix FPGAs and the VIPIC ASIC.

[0104] The user interface computer can be implemented as a computer on the same subnet as the detector head. The interface computer runs software that allows a user to control and configure the detector head and data acquisition system. The data acquisition system receives all of the data from the detector head and is responsible for storing and/or processes the data.

[0105] Based on the foregoing, it can be appreciated that a number of example embodiments, preferred and alternative, are disclosed herein. For example, in one embodiment, a detecting apparatus can be implemented which is composed of a multi-tier 3D integrated ASIC comprising at least one analog tier and at least one digital tier; a sensor bonded to the multi-tier 3D integrated ASIC; an electrical substrate; a plurality of FPGAs or custom data management ASICs; a thermal management system; a power distribution system; and a plurality of connectors to transfer data to a data acquisition system configured for radiation spectroscopy or imaging with zero suppressed or full frame readout.

[0106] In some example embodiments, the aforementioned electrical substrate can be a ceramic or a material based readout board. In another example embodiment, a dead-time-less operation can be provided, which continuously processes signals within user defined time frames. In some example embodiments, a segmented sensor can be implemented with a plurality of sensor pixels and a matching segmented analog tier with a plurality of analog pixels. Each analog pixel among the plurality of analog pixels can include one or more charge sensitive amplifiers with sensor leakage current compensation, and can also include, for example, a shaping filter, one or more comparators, and at least one trimming digital to analog converter (DAC). The at least one digital tier can be configured with a digital functionality for processing signals from the plurality of analog pixels of the at least one analog tier and transfers data off multi-tier 3D integrated ASIC.

[0107] In some example embodiments, the multi-tier 3D integrated ASIC can be die-to-wafer bonded to a sensor layer on one side and to the ceramic or a material based readout board on the other side to configure an assembly comprising a dead-zone-less detector module.

[0108] The dead-zone-less detector module can include a plurality of additional electrical components include at least one DAC that biases the multi-tier 3D integrated ASIC, and at least one decoupling capacitor, and which performs a plurality of functions including power distribution, control and clocks from FPGA to ASICs and data transfer from ASICs to FPGA. The dead-zone-less detector module can also be configured with a plurality of connectors that receive a plurality of signals including power, biases and clocks, and which transmits high speed, multiplexed and concentrated data to a detector head.

[0109] In some example embodiments, the aforementioned detector head can be configured to contain a plurality of detector modules, and a thermal management system for power dissipation placed in proximity to the plurality of detector modules. The detector head can transfer a large volume of high-speed data to a Data Acquisition (DAQ) system for further processing or storage of the data. The detector head can also include additional circuitry and components that allow the detector head to function as a data concentrator, receiving data from a plurality of ASICs processing the data and sending the data to the DAQ for further processing.

[0110] In an example embodiment, the multi-tier 3D integrated ASIC includes the at least one analog and the at least one digital tier, which are precisely diced, and then die-to-wafer bonded to a sensor layer on one side such that a resulting assembly constitutes either a dead-zone-less detector module or allows for a minimum gaps between ASICs.

[0111] In another example embodiment, a method of configuring a detecting apparatus can be implemented, which includes processing or fabrication steps such as, for example, providing an electrical substrate; providing a multi-tier 3D integrated ASIC comprising at least one analog tier and digital tier; bonding a sensor to the multi-tier 3D integrated ASIC; providing a plurality of FPGAs or custom data management ASICs: configuring a thermal management system; providing a power distribution system; and configuring a plurality of connectors to transfer data to a data acquisition system configured for radiation spectroscopy or imaging with zero suppressed or full frame readout.

[0112] In another example embodiment, processing or fabrication steps can be implemented, such as, for example: configuring the at least one analog tier and the at least one digital tier utilizing a CMOS process, and subsequently a face-to-face bonded operation; thinning the at least one digital tier to a few micrometers of Si; adding TSV in the at least one digital tier TSV and/or exposing previously buried TSV's, adding back metal pads to render connections to TSV's; adding a handle wafer covering up pads; flipping over an assembly and thinning the at least one analog tier to a few micrometers of Si; adding TSV in the at least one analog tier TSV or exposing previously buried TSV's; adding temporary metal pads to a periphery where test connections were pre-routed; testing a subset of analog and digital functionalities to verify a design as well as a successful 3D assembly to identify Known Good Dies (KGD); removing temporary pads; preparing a surface for back-to-face bonding of a back face of an analog and front face of a sensor; precisely dicing a 3D assembled wafer without destroying chip edges; utilizing KGD to die-to-wafer bonding to sensor with minimum gaps; removing handle material from a digital side to expose buried pads; flipping and bump-bonding to a ceramic or a material based board; flipping and bonding FPGAs on an opposite side; populating all other circuit components to create a detector module; and altering the order of bonding ASICs, FPGAs and other circuit to accommodate bonding requirements.

[0113] It can be appreciated that the example embodiments discussed and illustrated herein serve only as examples to illustrate several ways of implementation of the present disclosure. Such example embodiments should not be construed as to limit the spirit and scope of the present disclosure. It should be noted that those skilled in the art may still make various modifications or variations without departing from the spirit and scope of the disclosed example embodiments. Such modifications and variations shall fall within the protection scope of the embodiments, as defined in attached claims.

1. A detecting apparatus, comprising:
- a multi-tier 3D integrated ASIC comprising at least one analog tier and at least one digital tier;
- a sensor bonded to said multi-tier 3D integrated ASIC;
- an electrical substrate;
- a plurality of FPGAs or custom data management ASICs;
- a thermal management system;
- a power distribution system; and
- a plurality of connectors to transfer data to a data acquisition system configured for radiation spectroscopy or imaging with zero suppressed or full frame readout.

2. The apparatus of claim **1** wherein said electrical substrate comprises a ceramic or a material based readout board.

3. The apparatus of claim **1** comprising a dead-time-less operation that continuously processing signals within user defined time frames.

4. The apparatus of claim **1** further comprising a segmented sensor with a plurality of sensor pixels and a matching segmented analog tier with a plurality of analog pixels.

5. The apparatus of claim **4** wherein each analog pixel among said plurality of analog pixels includes at least a charge sensitive amplifier with sensor leakage current compensation, a shaping filter, at least one comparator, and at least one trimming digital to analog converter (DAC).

6. The apparatus of claim **4** wherein said at least one digital tier comprises a digital functionality for processing signals from said plurality of analog pixels of said at least one analog tier and transfers data off multi-tier 3D integrated ASIC.

7. The apparatus of claim **2** wherein said multi-tier 3D integrated ASIC is die-to-wafer bonded to a sensor layer on one side and to said ceramic or a material based readout board on the other side to configure an assembly comprising a dead-zone-less detector module.

8. The apparatus of claim **7** wherein said dead-zone-less detector module further comprises a plurality of additional electrical components include at least one DAC that biases said multi-tier 3D integrated ASIC, and at least one decoupling capacitor, and which performs a plurality of functions including power distribution, control and clocks from FPGA to ASICs and data transfer from ASICs to FPGA.

9. The apparatus of claim **7** wherein said dead-zone-less detector module comprises a plurality of connectors that receive a plurality of signals including power, biases and clocks, and which transmits high speed, multiplexed and concentrated data to a detector head.

10. The apparatus of claim **9** wherein said detector head contains a plurality of detector modules, and a thermal management system for power dissipation placed in proximity to said plurality of detector modules.

11. The apparatus of claim **9** wherein said detector head transfers a large volume of high-speed data to a Data Acquisition (DAQ) system for further processing or storage of said data.

12. The apparatus of claim **11** wherein said detector head includes additional circuitry and components that allow said detector head to function as a data concentrator, receiving data from a plurality of ASICs processing said data and sending said data to said DAQ for further processing.

12. The apparatus of claim **1** wherein said multi-tier 3D integrated ASIC comprises said at least one analog and said at least one digital tier, which are precisely diced, and then die-to-wafer bonded to a sensor layer on one side such that a resulting assembly constitutes either a dead-zone-less detector module or allows for a minimum gaps between ASICs.

13. A method of configuring a detecting apparatus, said method comprising:

providing an electrical substrate;

providing a multi-tier 3D integrated ASIC comprising at least one analog tier and digital tier;

bonding a sensor to said multi-tier 3D integrated ASIC;

providing a plurality of FPGAs or custom data management ASICs;

configuring a thermal management system;

providing a power distribution system; and

configuring a plurality of connectors to transfer data to a data acquisition system configured for radiation spectroscopy or imaging with zero suppressed or full frame readout.

14. The method of claim **13** further comprising:

configuring said at least one analog tier and said at least one digital tier utilizing a CMOS process, and subsequently a face-to-face bonded operation;

thinning said at least one digital tier to a few micrometers of Si;

adding TSV in said at least one digital tier TSV and/or exposing previously buried TSV's;

adding back metal pads to render connections to TSV's;

adding a handle wafer covering up pads;

flipping over an assembly and thinning said at least one analog tier to a few micrometers of Si;

adding TSV in said at least one analog tier TSV or exposing previously buried TSV's;

adding temporary metal pads to a periphery where test connections were pre-routed;

testing a subset of analog and digital functionalities to verify a design as well as a successful 3D assembly to identify Known Good Dies (KGD);

removing temporary pads;

preparing a surface for back-to-face bonding of a back face of an analog and front face of a sensor;

precisely dicing a 3D assembled wafer without destroying chip edges;

utilizing KGD to die-to-wafer bonding to sensor with minimum gaps;

removing handle material from a digital side to expose buried pads;

flipping and bump-bonding to a ceramic or a material based board;

flipping and bonding FPGAs on an opposite side;

populating all other circuit components to create a detector module; and

altering the order of bonding, ASICs, FPGAs and other circuit to accommodate bonding requirements.

15. The method of claim **13** wherein said electrical substrate comprises a ceramic or a material based readout board.

16. The method of claim **13** further comprising providing a dead-time-less operation that continuously processing signals within user defined time frames.

17. The method of claim **13** further comprising configuring a segmented sensor with a plurality of sensor pixels and a matching segmented analog tier with a plurality of analog pixels.

18. The method of claim **17** wherein each analog pixel among said plurality of analog pixels includes at least a charge sensitive amplifier with sensor leakage current compensation, a shaping filter, at least one comparator, and at least one trimming digital to analog converter (DAC).

19. The method of claim **17** further comprising configuring said at east one digital tier to comprise a digital functionality for processing signals from said plurality of analog pixels of said at least one analog tier and transfers data off multi-tier 3D integrated ASIC.

20. The method of claim **14** further comprising die-to-wafer bonding said multi-tier 3D integrated ASIC is die-to-wafer to a sensor layer on one side and to said ceramic or a material based readout board on the other side to configure an assembly comprising a dead-zone-less detector module.

21. The method of claim **20** further comprising configuring said dead-zone less detector module to further comprise a plurality of additional electrical components include at least one DAC that biases said multi-tier 3D integrated ASIC, and at least one decoupling capacitor, and which performs a plurality of functions including power distribution, control and clocks from FPGA to ASICs and data transfer from ASICs to FPGA.

22. The method of claim **20** further comprising configuring said dead-zone-less detector module to comprise a plurality of connectors that receive a plurality of signals

including power, biases and clocks, and which transmits high speed, multiplexed and concentrated data to a detector head.

23. The method of claim **22** further comprising configuring said detector head to contain a plurality of detector modules, and a thermal management system for power dissipation placed in proximity to said plurality of detector modules.

24. The method of claim **22** further comprising configuring said detector head to transfer a large volume of high-speed data to a Data Acquisition (DAQ) system for further processing or storage of said data.

25. The method of claim **24** further comprising configuring said detector head to include additional circuitry and components that allow said detector head to function as a data concentrator, receiving data from a plurality of ASICs processing said data and sending said data to said DAQ for further processing.

26. The method of claim **13** further comprising configuring said multi-tier 3D integrated ASIC to comprise said at least one analog and said at least one digital tier, which are precisely diced, and then die-to-wafer bonded to a sensor layer on one side such that a resulting assembly constitutes either a dead-zone-less detector module or allows for a minimum gaps between ASICs.

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