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(54) METHOD FOR RECOGNIZING ORDER OF SIGNALS

(57) A method for recognizing an order of signals by means of a main MUTEX circuit is characterized in that metastability of the main MUTEX circuit (MM_x) is detected and is signaled by means of an additional MUTEX circuit (MA_x). If metastability of the main MUTEX circuit (MM_x) is detected, default values are assigned to an appropriate bit group of an output digital word (B) by means of an output module (OM).

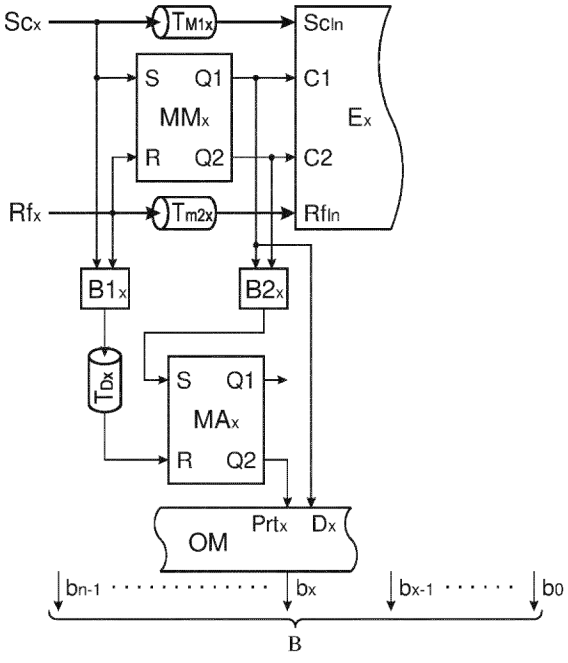

Fig. 1.

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Description

[0001] The subject of the invention is a method for recognizing an order of signals that can be applied in control and measurement systems and automation, but mainly in analog-to-digital conversion of the TDC type (time-to-digital conversion), in which the analog input quantity is a time interval. TDC converters of this type are used e.g. in: laser rangefinders, digital phase locked loops (DPLL), positron emission tomography and post-production tests of time parameters of very large-scale integration (VLSI) integrated circuits.

[0002] From the publication: M. A. Abas, G. Russell and D. J. Kinniment, "Design of Sub-10-Picoseconds On-Chip Time Measurement Circuit" a method for recognizing an order of signals by means of a MUTEX circuit (mutual exclusion) is known. In this method, a source signal is fed to a set input of the MUTEX circuit, whereas a reference signal is fed to a reset input of the MUTEX circuit. The one of the mentioned signals that will be first to enter its active state, will be indicated as a leading signal by means of the MUTEX circuit. One of the two outputs of the MUTEX circuit that corresponds to this signal will be then put into active state, confirming that the order of signals was finally settled. The active state of the other of the signals that reaches the MUTEX circuit will not affect the state of the outputs of this system.

[0003] From the publication: M. A. Abas, G. Russell and D. J. Kinniment, "Built-in time measurement circuits - a comparative design study" IET Comput. Digit. Tech., 2007, 1, (2), pp. 87 - 97 a method of analog-to-digital conversion of the TDC type (time-to-digital conversion) is known, in which the coded analog quantity is a time interval. This interval is represented by a distance of time between the moments in which a source signal and a reference signal successively enter their active states. An amount of the measured interval is determined by means of the successive approximation method and finally presented in the form of an n-bit output digital word. The processing is carried out in a system composed of n sequentially connected cells. Each of the cells first waits until active state appears on one of its signal inputs, which means that the leading one of the signals has just reached this cell. A reference delay is then introduced into the leading signal path, which is twice as small as the reference delay introduced by the previous cell and simultaneously twice as large as the reference delay introduced by the next cell. However, the given cell does not introduce the reference delay into the path of the second, later signal. Furthermore, each of the cells, based on the path configuring method of both signals it has introduced, assigns an appropriate value to a bit having index x of the n-bit output digital word, wherein the position of a given bit having index x in the digital word corresponds to the location of the considered cell in the converter structure. The processing ultimately leads to the alignment in time of the moments in which both signals enter active state. This alignment can be achieved with an accuracy not worse than the absolute resolution of a given converter. The absolute value of the measured time interval can therefore also be determined as a difference of sums of reference delays introduced into the paths of each signal.

[0004] The order in which the active states of the source signal and of the reference signal reach a given cell are recognized by means of a MUTEX circuit. Occurrence of the leading active state on one of the two inputs of this circuit causes the corresponding of its two outputs to enter active state. These outputs control the configuration of two multiplexers. By using them, the reference delay is introduced into the path of the leading signal and simultaneously it is not introduced into the path of the second, later signal. However, since the propagation times of information through the MUTEX circuit and each of the multiplexers are non-zero, in the paths of both signals in each cell of the converter delay elements are permanently included, by means of which the influence of the propagation delays of the mentioned elements is compensated.

[0005] From the publication: D. J. Kinniment, O. V. Maevsky, A. Bystrov, G. Russell and A. V. Yakovlev, "On-Chip structures for Timing Measurement and Test" a metastability effect of a MUTEX circuit is known. This circuit is characterized by a constant and small propagation delay in a situation where active states on both its inputs do not appear quasi-simultaneously. However, if both inputs of the MUTEX circuit enter their active states quasi-simultaneously, the response time of the MUTEX circuit increases rapidly. In this situation, long after entering active states by both inputs of the MUTEX circuit, both of its outputs still remain inactive. This effect cannot be fully compensated for by the delays permanently included in the paths of both signals, because the absolute value of the inaccuracy of each of such large delays, resulting from the dispersion of technological processes, becomes significantly greater than the resolution of the converter, falsifying the results of each of the measurements performed. Thus, in the case of metastability of the MUTEX circuit, which however does not happen often, the active signal finally appears on one of the outputs of this circuit with a large and uncompensated delay. This delay makes it impossible to properly configure further parts of the paths of both signals before the active states of these signals reach the considered parts. As a result of the above, at a given stage of processing, none of the signal paths will contain the required reference delay or, in another implementation of the converter, the paths of both signals will contain the same reference delay. In both cases, the processing result will be burdened with an error, the value of which may reach even half of the processing range, depending on the stage of processing where metastability phenomenon occurs.

[0006] A method for recognizing an order of signals according to the invention consists in detecting, by means of a main MUTEX circuit, executed during an analog-to-digital conversion step used to determine a value

of a bit having index x of an n-bit output digital word, that a source signal was the first to enter its active state, or that a reference signal was the first to enter its active state. A path configuration circuit is signaled by means of a first output of the main MUTEX circuit that the source signal was the first to enter its active state. The path configuration circuit is signaled by means of a second output of the main MUTEX circuit that the reference signal was the first to enter its active state. The source signal is fed by means of a first delay circuit to an input of a source path of the path configuration circuit. Simultaneously the reference signal is fed by means of a second delay circuit to an input of a reference path of the path configuration circuit. Propagation time of the first delay circuit is equal to propagation time of the second delay circuit and is longer than a nominal propagation delay of the main MUTEX circuit.

[0007] The essence of the solution lies in that metastability of the main MUTEX circuit is detected by means of an additional MUTEX circuit, by controlling the delay with which the first output of the main MUTEX circuit or the second output of the main MUTEX circuit is put into active state by means of the main MUTEX circuit. This delay refers to the moment in which the source signal was the first to enter its active state or the reference signal was the first to enter its active state. The metastability of the main MUTEX circuit is signaled by means of the additional MUTEX circuit by bringing a second output of the additional MUTEX circuit into active state. Entering active state by the source signal or entering active state by the reference signal is detected by means a first gate and is signaled by means of an additional delay circuit to the additional MUTEX circuit, bringing a reset input of the additional MUTEX circuit into active state. Propagation time of the additional delay circuit is shorter than the propagation time of the first delay circuit and simultaneously is longer than the nominal propagation delay of the main MUTEX circuit. Entering active state by the first output of the main MUTEX circuit or entering active state by the second output of the main MUTEX circuit is detected and is signaled by means of a second gate to the additional MUTEX circuit, bringing a set input of the additional MUTEX circuit into active state. To the bit having index x of the n-bit output digital word a value is assigned by means of an output module in the following manner. If during the analog-to-digital conversion step used to determine the value of the bit having index x of the n-bit output digital word, metastability of the main MUTEX circuit is signaled by means of the additional MUTEX circuit and a priority input of the output module is put into active state by means of the second output of the additional MUTEX circuit, then to the bit having index x and to all possible less significant bits of the n-bit output digital word default logical states are assigned by means of the output module. Simultaneously, the state indicated by means of the first output of the main MUTEX circuit to a data input of the output module is ignored by the output module during this and any subsequent analog-to-digital conversion steps. If, however, during the analog-to-digital conversion step used to determine the value of the bit having index x of the n-bit output digital word, metastability of the main MUTEX circuit is not signaled by means of the additional MUTEX circuit and the priority input of the output module is kept by the second output of the additional MUTEX circuit in inactive state and metastability is not signaled during any of possible earlier analog-to-digital conversion steps used to determine values of more significant bits of the n-bit output digital word, then to the bit having index x of the n-bit output digital word a logical state according to the state of the data input of the output module is assigned by means of the output module. Thus, if the data input of the output module is put into active state by means of the first output of the main MUTEX circuit, then to the bit having index x of the n-bit output digital word a logical state one is assigned by means of the output module. Otherwise, when the data input of the output module is kept in inactive state by means of the first output of the main MUTEX circuit, to the bit having index x of the n-bit output digital word a logical state zero is assigned by means of the output module.

[0008] It is advantageous if the active state of the source signal, of the reference signal, of the first output of the main MUTEX circuit and of the second output of the main MUTEX circuit as well as of a first output of the additional MUTEX circuit and of the second output of the additional MUTEX circuit is a logical high state. Then, by means of the first gate and by means of the second gate a logical OR function is implemented.

[0009] It is also advantageous if the active state of the source signal, of the reference signal, of the first output of the main MUTEX circuit and of the second output of the main MUTEX circuit as well as of the first output of the additional MUTEX circuit and of the second output of the additional MUTEX circuit is a logical low state. Then, by means of the first gate and by means of the second gate a logical AND function is implemented.

[0010] It is advantageous if the default logical states are assigned by means of the output module to selected bits of the n-bit output digital word in such a way that to the bit having index x of the n-bit output digital word a logical state zero is assigned by means of the output module. Simultaneously, to all possible less significant bits of the n-bit output digital word logical states one are assigned by means of the output module.

[0011] It is also advantageous if the default logical states are assigned by means of the output module to selected bits of the n-bit output digital word in such a way that to the bit having index x of the n-bit output digital word a logical state one is assigned by means of the output module. Simultaneously, to all possible less significant bits of the n-bit output digital word logical states zero are assigned by means of the output module.

[0012] The advantage of the solution lies in ensuring the correct operation of the TDC-type analog-to-digital converter even in a situation where metastability of the MUTEX circuit occurs at any stage of processing. In such

a situation, to all bits of this part of the output digital word which due to the metastability of the MUTEX circuit is at risk of being falsified, a predetermined default value will be assigned. The final value of the output digital word obtained in this way differs by at most one from the result that could be obtained in an ideal, completely metastability-free converter.

[0013] The solution also allows to interrupt the analog-to-digital conversion process, during which metastability of the MUTEX circuit occurred. In this way both the time and the amount of energy necessary to obtain the correct processing result are reduced.

[0014] The subject of the invention is explained in exemplary embodiments in the drawing which shows:

Fig. 1 - a diagram of a system for recognizing an order of signals.

Fig. 2 - a diagram of a MUTEX circuit reacting to an active state in the form of a logical high state, containing an asynchronous RS flip-flop composed of NAND logic gates and a simple filter.

Fig. 2 - a diagram of a MUTEX circuit reacting to an active state in the form of a logical low state, containing an asynchronous RS flip-flop composed of NOR logic gates and an inverted filter.

Fig. 4 - a time interval ΔT separating moments of entering active states by a source signal Sc_x and by a reference signal Rf_x.

Fig. 5 - a propagation delay t_P of the main MUTEX circuit MM_x as a function of time interval ΔT.

[0015] According to the invention, a method for recognizing an order of signals consists in detecting, by means of a main MUTEX circuit MM_x, which of two signals reaches earlier a cell used to determine a value of a bit having index x, b_x, of an n-bit output digital word B in a TDC-type analog-to-digital converter, using the successive approximation method. The first of the signals controlled by means of the main MUTEX circuit MM_x is a source signal Sc_x, whereas the second signal is a reference signal Rf_x. The arrival of the leading signal to the considered cell of the analog-to-digital converter is recognized by means of a set input S of the main MUTEX circuit MM_x or by a reset input R of the main MUTEX circuit MM_x, put into active state by means of, respectively, the source signal Sc_x or the reference signal Rf_x. In this exemplary solution the active state is represented by a logical high state. An appearance of the leading signal is signaled to a path configuration circuit E_x by means of a first output Q1 of the main MUTEX circuit MM_x, if the leading signal is the source signal Sc_x, or by means of a second output Q2 of the main MUTEX circuit MM_x, if the leading signal is the reference signal Rf_x. A propagation delay t_P of the main MUTEX circuit MM_x is compensated in excess for the source signal Sc_x and for the reference signal Rf_x by means of, respectively, a first delay circuit T_{M1x} and a second delay circuit T_{M2x}. Propagation time t_M of the first delay circuit T_{M1x} is equal to propagation time t_M of the second delay circuit T_{M2x} and is five times longer than a nominal propagation delay t_N of the main MUTEX circuit MM_x. Thereby, in the absence of metastability of the main MUTEX circuit MM_x it is guaranteed, by means of the first delay circuit T_{M1x} and the second delay circuit T_{M2x}, that the source signal Sc_x and the reference signal Rf_x will reach, respectively, an input of a signal path Sc_{In} of the path configuration circuit E_x and an input of a reference path Rf_{In} of the path configuration circuit E_x only after the path configuration circuit E_x has been signaled by means of the main MUTEX circuit MM_x, which of these signals is the leading one. In this exemplary solution the active state of the first output Q1 of the main MUTEX circuit MM_x and of the second output Q2 of the main MUTEX circuit MM_x as well as of a first output Q1 of an additional MUTEX circuit MA_x and of a second output Q2 of the additional MUTEX circuit MM_x is a logical high state.

[0016] The metastability of the main MUTEX circuit MM_x is detected by means of the additional MUTEX circuit MA_x, by comparing the propagation delay t_P of the main MUTEX circuit MM_x with propagation time to of an additional delay circuit T_{Dx}. The propagation time to of the additional delay circuit T_{Dx} is four times longer than the nominal propagation delay t_N of the main MUTEX circuit MM_x and is shorter than the propagation time t_M of the first delay circuit T_{M1x} and of the second delay circuit T_{M2x}. The beginning of an interval of the propagation delay t_P of the main MUTEX circuit MM_x is detected by means of a first gate $B1_x$ acting in this exemplary solution as a logical sum, is delayed by means of the additional delay circuit T_{Dx} and is signaled to the additional MUTEX circuit MA_x by means of a reset input R of the additional MUTEX circuit MA_x. The end of the interval of the propagation delay t_P of the main MUTEX circuit MM_x is detected by means of a second gate $B2_x$ acting in this exemplary solution as a logical sum and is signaled to the additional MUTEX circuit MA_x by means of a set input S of the additional MUTEX circuit MA_x. If the interval of the propagation delay t_P of the main MUTEX circuit MM_x is longer than the propagation time to of the additional delay circuit T_{Dx}, then the detected metastability of the main MUTEX circuit MM_x is signaled by means of the additional MUTEX circuit MA_x to an output module OM, bringing a priority input Prt_x of the output module OM into active state by means of the second output Q2 of the additional MUTEX circuit MA_x.

[0017] If the metastability of the main MUTEX circuit MM_x is detected by means of the additional MUTEX circuit MA_x in the cell of the analog-to-digital converter used to determine a value of the bit having index x, b_x, of the n-bit output digital word B, to the bit having index x, b_x, and to all possible less significant bits b_{x-1}, ..., bo of the n-bit output digital word B default logical states are assigned by means of the output module OM. In this exemplary solution, to the bit having index x, b_x, of the n-bit output digital word B a logical state zero is assigned by

means of the output module OM, and to all possible less significant bits b_{x-1}, ..., b_0 of the n-bit output digital word B logical states one are assigned by means of the output module OM. Simultaneously, the state indicated by means of the first output Q1 of the main MUTEX circuit MM_x to a data input D_x of the output module OM is ignored by means of the output module OM. In such case the output module OM ignores also the states indicated to the data input of the output module OM in all possible subsequent cells of the analog-to-digital converter, used to determine values of less significant bits b_x, ..., b_0 of the n-bit output digital word B.

[0018] If no metastability of the main MUTEX circuit MM_x is detected by means of the additional MUTEX circuit MA_x in the cell of the analog-to-digital converter used to determine a value of the bit having index x, b_x, of the n-bit output digital word B and provided that no metastability is detected in any of the cells of the analog-to-digital converter, used to determine values of more significant bits b_{n-1}, ..., b_{x+1} of the n-bit output digital word B, to the bit having index x, b_x, of the n-bit output digital word B a logical state according to the state of the data input D_x of the output module OM is assigned by means of the output module OM. If the data input D_x of the output module OM is put into active state by means of the first output Q1 of the main MUTEX circuit MM_x, to the bit having index x, b_x, of the n-bit output digital word B a logical state one is assigned by means of the output module OM. Otherwise, when the data input D_x of the output module OM is kept in inactive state by means of the first output Q1 of the main MUTEX circuit MMx, to the bit having index x, b_x, of the n-bit output digital word B a logical state zero is assigned by means of the output module OM.

[0019] Another method for recognizing an order of signals, according to the invention, differs from the previous one in that the active state of the source signal Sc_x and the active state of the reference signal Rf_x is represented by a logical low state. The active state of the first output Q1 of the main MUTEX circuit MM_x and of the second output Q2 of the main MUTEX circuit MM_x as well as of the first output Q1 of the additional MUTEX circuit MA_x and of the second output Q2 of the additional MUTEX circuit MM_x is also a logical low state. Moreover, the first gate $B1_x$ and the second gate $B2_x$ function as a logical product in this exemplary solution.

[0020] A further method for recognizing an order of signals, according to the invention, differs from the previous ones in that, if to selected bits of the n-bit output digital word B the default logical states are assigned by means of the output module OM, starting from the bit having index x, b_x, then to the bit having index x, b_x, of the n-bit output digital word B a logical state one is assigned by means of the output module OM, and to all possible less significant bits b_{x-1}, ..., b_0 of the n-bit output digital word B logical states zero are assigned by means of the output module OM.

[0021] According to the invention, a system for recognizing an order of signals, in a first exemplary solution (fig. 1), in a cell of an analog-to-digital converter, used to determine a value of a bit having index x, b_x, of an n-bit output digital word B, comprises a main MUTEX circuit MM_x. The main MUTEX circuit MM_x is provided with a set input S, a reset input R, a first output Q1 and a second output Q2. The set input S of the main MUTEX circuit MM_x is connected to an input of a source signal Sc_x, and the reset input R of the main MUTEX circuit MM_x is connected to an input of a reference signal Rf_x. The first output Q1 of the main MUTEX circuit MM_x is connected to a first control input C1 of a path configuration circuit E_x, whereas the second output Q2 of the main MUTEX circuit MM_x is connected to a second control input C2 of the path configuration circuit E_x. The input of the source signal Sc_x is furthermore connected to an input of a first delay circuit T_{M1x}, whose output is connected to an input of a source path Sc_{In} of the path configuration circuit E_x. On the other hand, the input of the reference signal Rf_x is connected to an input of a second delay circuit T_{M2x}, whose output is connected to an input of a reference path Rf_{In} of the path configuration circuit E_x. Propagation time t_M of the first delay circuit T_{M1x} is equal to propagation time t_M of the second delay circuit T_{M2x} and is five times longer than a nominal propagation delay t_N of the main MUTEX circuit MM_x. The input of the source signal Sc_x is connected to a first input of a first gate $B1_x$, whose second input is connected to the input of the reference signal Rf_x. An output of the first gate $B1_x$ is in turn connected to an input of an additional delay circuit T_{Dx}, whose output is connected to a reset input R of an additional MUTEX circuit MA_x. Propagation time to of the additional delay circuit T_{Dx} is four times longer than the nominal propagation delay t_N of the main MUTEX circuit MM_x and is shorter than the propagation time t_M of the first delay circuit T_{M1x} and of the second delay circuit T_{M2x}. In this exemplary system the main MUTEX circuit MM_x and the additional MUTEX circuit MA_x are known MUTEX circuits including asynchronous RS flip-flops composed of NAND logic gates and simple filters (fig.2). The first output Q1 of the main MUTEX circuit MM_x is connected to a data input D_x of an output module OM and to a first input of a second gate $B2_x$, whose second input is connected to the second output Q2 of the main MUTEX circuit MM_x. An output of the second gate $B2_x$ is in turn connected to a set input S of the additional MUTEX circuit MA_x, whose second output Q2 is connected to a priority input Prt_x of the output module OM. The output module OM is furthermore provided with outputs of bits b_{n-1}, ..., bo of the n-bit output digital word B. In this exemplary system, the first gate $B1_x$ and the second gate $B2_x$ are OR logic gates.

[0022] In a second exemplary solution, the system for recognizing an order of signals according to the invention differs from the first one in that the main MUTEX circuit MM_x and the additional MUTEX circuit MA_x are known MUTEX circuits including asynchronous RS flip-flops composed of NOR logic gates and inverted filters (fig. 3).

Moreover, in this exemplary solution, the first gate $B1_x$ and the second gate $B2_x$ are AND logic gates.

[0023] Recognition of an order of signals implemented, according to the invention, in the first exemplary system (fig. 1) proceeds as follows. The MUTEX circuit indicates, as the leading signal, the signal which enters its active state earlier. It happens so, however, provided that both signals do not enter their active states quasi-simultaneously. The first of the considered signals is the source signal Sc_x, and the second is the reference signal Rf_x. In the first exemplary system the active state is a logical high state.

[0024] In the case where the source signal Sc_x and the reference signal Rf_x do not enter their active states quasi-simultaneously, a time interval ΔT separating activation moments of these signals (fig. 4) has little effect on length of a propagation delay t_P (fig. 5) with which the main MUTEX circuit MM_x reacts on the appearance of the leading signal by activating one of its two outputs. The propagation delay of the main MUTEX circuit MM_x in such case is equal or slightly larger than the nominal propagation delay t_N of the main MUTEX circuit MM_x (fig. 5) and is shorter than the propagation time to of the additional delay circuit T_{Dx} (fig. 5). If the leading signal is the source signal Sc_x, then the first output Q1 of the main MUTEX circuit MM_x will be put into active state. If, however, the leading signal is the reference signal Rf_x, then the second output Q2 of the main MUTEX circuit MM_x will be put into active state. Later entering active state by the second of the signals has no influence on the already established state of the outputs of the main MUTEX circuit MM_x. In the case where the leading signal is the source signal Sc_x, the active state of the first output Q1 of the main MUTEX circuit MM_x, fed to the first control input C1 of the path configuration circuit E_x causes a reference delay, having length suitable for a given analog-to-digital converter cell, to be included in a path of the source signal Sc_x. Simultaneously, a path of the reference signal Rf_x will not include the reference delay. Otherwise, when the leading signal is the reference signal Rf_x, the active state of the second output Q2 of the main MUTEX circuit MM_x, fed to the second control input C2 of the path configuration circuit E_x, causes the reference delay to be included in the path of the reference signal Rf_x. Simultaneously, the path of the source signal SC_x will not include the reference delay. The source signal Sc_x and the reference signal Rf_x are fed to, respectively, the input of the source path Sc_{In} of the path configuration circuit E_x and the input of the reference path Rf_{In} of the path configuration circuit E_x through the first delay circuit T_{M1x} and the second delay circuit T_{M2x}, respectively. In the considered case the propagation delay t_P of the main MUTEX circuit MM_x is shorter than the propagation times t_M of the first delay circuit T_{M1x} and of the second delay circuit T_{M2x} (fig. 5). Therefore, each of the signals reaches the input of its own path in the path configuration circuit E_x only when both paths have been previously properly configured, what is necessary for proper operation of the analog-to-digital converter.

[0025] The length of the propagation delay t_P of the main MUTEX circuit MM_x is always controlled by means of the additional MUTEX circuit MA_x. The beginning of an interval of the propagation delay t_P of the main MUTEX circuit MM_x is indicated by means of the first gate $B1_x$, whose output enters active state as a result of the appearance of the leading signal at either of the two inputs of this gate. An output signal of the first gate $B1_x$ is delayed by means of the additional delay circuit T_{Dx} and eventually reaches the reset input R of the additional MUTEX circuit MA_x. The end of the interval of the propagation delay t_P of the main MUTEX circuit MM_x is indicated by means of the second gate $B2_x$, whose output enters active state as a result of the appearance of the active state at either of the two outputs of the main MUTEX circuit MM_x. An output signal of the second gate $B2_x$ is fed to the set input S of the additional MUTEX circuit MA_x. Propagation delays of the first gate $B1_x$ and of the second gate $B2_x$ are identical and compensate each other. The propagation delay t_P of the main MUTEX circuit MM_x is in turn, in the considered case, shorter than the propagation time to of the additional delay circuit T_{Dx} (fig. 5). Therefore, the set input S of the additional MUTEX circuit MA_x will be put into active state first. Thereby, the active state will eventually appear on an unused first output Q1 of the additional MUTEX circuit MA_x. The second output Q2 of the additional MUTEX circuit MA_x will remain in inactive state also when the active state of the additional delay circuit T_{Dx} eventually reaches the reset input R of the additional MUTEX circuit MA_x. Thereby the priority input Prt_x of the output module OM will be constantly kept in inactive state and will not affect in any way the value given to the bit b_x by the output module OM. The value of this bit will be only influenced by the state of the first output Q1 of the main MUTEX circuit MM_x, fed to the data input D_x of the output module OM. If the data input D_x of the output module OM is in inactive state, then a logical state zero is assigned to the bit b_x by means of the output module OM. Otherwise, when the data input D_x of the output module OM is in active state, a logical state one is assigned to the bit b_x by means of the output module OM.

[0026] In the case where the source signal Sc_x and the reference signal Rf_x enter their active states quasi-simultaneously, the main MUTEX circuit MM_x exhibits metastability. The propagation delay t_P of the main MUTEX circuit MM_x rapidly increases (fig. 5) and becomes longer than the propagation time to of the additional delay circuit T_{Dx}. The propagation delay t_P of the main MUTEX circuit MM_x may then become longer than the propagation time t_M of the first delay circuit T_{M1x} and of the second delay circuit T_{M2x} (fig. 5). In such case the source signal Sc_x and the reference signal Rf_x reach the input of the source path Sc_{In} of the path configuration circuit E_x and the input of the reference path Rf_{In} of the path configuration circuit E_x, respectively, even before the active state appears on one of the outputs of the main MUTEX circuit MM_x. Quasi-

simultaneous: the source signal Sc_x and the reference signal Rf_x therefore propagate through paths which have not yet been properly configured by means of the path configuration circuit E_x. Analog-to-digital conversion algorithm of the successive approximation method does not anticipate such a situation, and its occurrence causes falsification of the correct value of the determined output digital word B. At the same time, however, quasi-simultaneity of the source signal Sc_x and of the reference signal Rf_x means that in the previously performed steps of processing the positions of both signals have been already managed to align in the time domain, in addition, with an accuracy better than the resolution of a given converter. This situation can only occur when the measured time interval ΔT was initially quasi-equal to 1/2 of the processing range, or 1/4 of the processing range, or 3/4 of the processing range, or 1/8 of the processing range, etc.

[0027] So if the ideal analog-to-digital converter in which the main MUTEX circuit MM_x is completely metastability-free, encountered quasi-simultaneity of the source signal Sc_x and of the reference signal Rf_x in a processing step used to determine the bit having index x b_x, then such a converter in this processing step would include the reference delay in a path of one of the signals, and in each of subsequent processing steps it would include the reference delays of twice decreasing lengths in a path of the second of the signals, trying to realign the positions of these signals in time domain. Therefore it is certain that in the output digital word B of the ideal analog-to-digital converter, values of the bit b_x and of all possible less significant bits b_{x-1}, ..., b_0 must take one of two sequences: 0, 1, 1, ..., 1 or 1, 0, 0, ..., 0. Moreover, in case the source signal Sc_x and the reference signal Rf_x enter their active state simultaneously, both of the above sequences are equally likely. In the considered case, the result of analog-to-digital conversion can therefore be predicted with an accuracy to one, without carrying out the remaining steps of this process or omitting their results, which will turn out to be falsified for the real converter anyway due to metastability of the MUTEX circuit.

[0028] The metastability of the main MUTEX circuit MM_x is detected and signaled by means of the additional MUTEX circuit MA_x. In the considered case the propagation delay t_P of the main MUTEX circuit MM_x is longer than the propagation time t_M of the additional delay circuit T_{Dx} (fig. 5). Therefore, the reset input R of the additional MUTEX circuit MA_x will be put into active state first. Thereby, the active state will appear on the second output Q2 of the additional MUTEX circuit MA_x and will be forwarded to the priority input Prt_x of the output module OM, signaling the metastability of the main MUTEX circuit MM_x to the output module OM. As a result of the above, the output module OM will immediately assign default values to the bit b_x and to all possible less significant bits b_{x-1}, ..., b_0 of the output digital word B. Moreover, starting from this point of time, the output module OM will ignore the state of its data input D_x, both at that processing stage and at any subsequent processing stage. The output module OM will therefore assign a logical state zero to the bit b_x, and the output module OM will assign logical states one to all possible less significant bits b_{x-1}, ..., b_0 of the output digital word B. The final value of the output digital word B will be equal to or one less than the value of the output digital word B, which would be obtained in an ideal analog-to-digital converter. In another exemplary solution, the output module OM will assign a logical state one to the bit b_x, and the output module OM will assign logical states zero to all possible less significant bits b_{x-1}, ..., b_0 of the output digital word B. In this solution, the final value of the output digital word B will therefore be equal to or one greater than the value of the output digital word B, which would be obtained in an ideal analog-to-digital converter.

[0029] In a particular case the propagation delay t_P of the main MUTEX circuit MM_x is quasi-equal to the propagation time to of the additional delay circuit T_{Dx} (fig. 5). The propagation delay t_P of the main MUTEX circuit MM_x is therefore shorter than the propagation times t_M of the first delay circuit T_{M1x} and the second delay circuit T_{M2x} (fig. 5). Therefore, the source signal Sc_x and the reference signal Rf_x reach the input of the source path Sc_{In} of the path configuration circuit E_x and the input of the reference path Rf_{In} of the path configuration circuit E_x, respectively, only when the main MUTEX circuit MM_x has already put the appropriate control input of the path configuration circuit E_x into the active state. The source signal Sc_x and the reference signal Rf_x therefore propagate through paths configured properly and in advance as required. So the analog-to-digital conversion process is working properly, and the output module OM can use the state of the first output Q1 of the main MUTEX circuit MM_x to assign the appropriate value to the bit having index x, b_x, of the output digital word B.

[0030] As in any case, the length of the propagation delay t_P of the main MUTEX circuit MM_x is controlled by means of the additional MUTEX circuit MA_x. In the particular case under consideration, the propagation delay t_P of the main MUTEX circuit MM_x is quasi-equal to the propagation time to of the additional delay circuit T_{Dx} (fig. 5). Therefore, the set input S of the additional MUTEX circuit MA_x and the reset input R of the additional MUTEX circuit MA_x are put into their active states quasi-simultaneously, causing metastability of the additional MUTEX circuit MA_x. The result of it is a significant extension of the propagation delay of the additional MUTEX circuit MA_x and the inability to unambiguously indicate the output of the additional MUTEX circuit MA_x, which will eventually be put into active state. If the active state appears on the unused first output Q1 of the additional MUTEX circuit MA_x, the priority input Prt_x of the output module OM will still be kept in inactive state by means of the second output Q2 of the additional MUTEX circuit MA_x. The values of the bit having index x, b_x, and of a part of possible less significant bits b_{x-1}, b_{x-2}, ..., of the output digital word B, already determined as a result of the an-

alog-to-digital conversion process, which is still running correctly, will therefore be kept. If, however, the active state eventually appears on the second output Q2 of the additional MUTEX circuit MA_x, then the priority input Prt_x of the output module OM will be put into active state, signaling potential metastability of the main MUTEX circuit MM_x to the output module OM. As a result of the above, the output module OM will assign default values to the bit b_x and to all possible less significant bits b_{x-1}, ..., b_0 of the output digital word B. Moreover, the output module OM will ignore the state of its data input D_x, both at that processing stage and at any subsequent processing stage. The output module OM will therefore assign a logical state zero to the bit b_x, and the output module OM will assign logical states one to all possible less significant bits b_{x-1}, ..., b_0 of the output digital word B. The value of the output digital word B obtained in this way will be equal to or one less than the value of the output digital word B, that would be obtained by continuing the normal analog-to-digital conversion process. In another exemplary solution, the output module OM will assign a logical state one to the bit b_x, and the output module OM will assign logical states zero to all possible less significant bits b_{x-1}, ..., b_0 of the output digital word B. In this solution, the final value of the output digital word B will therefore be equal to or one greater than the value of the output digital word B, that would be obtained by continuing the normal analog-to-digital conversion process.

[0031] Recognition of an order of signals implemented, according to the invention, in the second exemplary system proceeds in an identical manner as in the first exemplary system (fig. 1), with the only difference that the active state is a logical low state.

Claims

1. A method for recognizing an order of signals, consisting in detecting, by means of a main MUTEX circuit, executed during an analog-to-digital conversion step used to determine a value of a bit having index x of an n-bit output digital word, that a source signal was the first to enter its active state, or that a reference signal was the first to enter its active state, and signaling by means of a first output of the main MUTEX circuit to a path configuration circuit that the source signal was the first to enter its active state, or signaling by means of a second output of the main MUTEX circuit to the path configuration circuit, that the reference signal was the first to enter its active state, wherein the source signal is fed by means of a first delay circuit to an input of a source path of the path configuration circuit and simultaneously the reference signal is fed by means of a second delay circuit to an input of a reference path of the path configuration circuit, wherein propagation time of the first delay circuit is equal to propagation time of the second delay circuit and is longer than a nominal propagation delay of the main MUTEX circuit, **characterized in that** metastability of the main MUTEX circuit (MM_x) is detected by means of an additional MUTEX circuit (MA_x), by controlling the delay with which the first output (Q1) of the main MUTEX circuit (MM_x) or a second output (Q2) of the main MUTEX circuit (MM_x) is put into active state by means of the main MUTEX circuit (MM_x), relative to the time in which the source signal (Sc_x) was the first to enter its active state or the reference signal (Rf_x) was the first to enter its active state, wherein the metastability of the main MUTEX circuit (MM_x) is signaled by means of the additional MUTEX circuit (MA_x) by bringing a second output (Q2) of the additional MUTEX circuit (MAx) into active state, whereas entering active state by the source signal (Sc_x) or entering active state by the reference signal (Rf_x) is detected by means of a first gate ($B1_x$) and is signaled by means of an additional delay circuit (T_{Dx}) to the additional MUTEX circuit (MA_x), bringing a reset input (R) of the additional MUTEX circuit (MA_x) into active state, wherein propagation time (to) of the additional delay circuit (T_{Dx}) is shorter than the propagation time (t_M) of the first delay circuit (t_{M1x}) and simultaneously is longer than the nominal propagation delay (t_N) of the main MUTEX circuit (MM_x), whereas entering active state by the first output (Q1) of the main MUTEX circuit (MMx) or entering active state by the second output (Q2) of the main MUTEX circuit (MM_x) is detected and is signaled by means of a second gate ($B2_x$) to the additional MUTEX circuit (MA_x), bringing a set input (S) of the additional MUTEX circuit (MA_x) into active state, whereas to the bit having index x (b_x) of the n-bit output digital word (B) a value is assigned by means of an output module (OM) in such a way that if during the analog-to-digital conversion step used to determine the value of the bit having index x (b_x) of the n-bit output digital word (B) metastability of the main MUTEX circuit (MM_x) is signaled by means of the additional MUTEX circuit (MA_x) and a priority input (Prt_x) of the output module (OM) is put into active state by means of the second output (Q2) of the additional MUTEX circuit (MA_x), then to the bit having index x (b_x) and to all possible less significant bits (b_{x-1}, ..., b_0) of the n-bit output digital word (B) default logical states are assigned by means of the output module (OM) and simultaneously the state indicated by means of the first output (Q1) of the main MUTEX circuit (MM_x) to a data input (D_x) of the output module (OM) is ignored by the output module (OM) during this and any subsequent analog-to-digital conversion steps, if, however, during the analog-to-digital conversion step used to determine the value of the bit having index x (b_x) of the n-bit output digital word (B) metastability of the main MUTEX circuit (MMx) is not signaled by means of the additional MUTEX circuit (MA_x) and the priority input (Prt_x) of the output module (OM) is kept in in-

active state by means of the second output (Q2) of the additional MUTEX circuit (MA_x) and metastability is not signaled during any of possible earlier analog-to-digital conversion steps used to determine values of more significant bits (b_{n-1}, ..., b_{x+1}) of the n-bit output digital word (B), then to the bit having index x (b_x) of the n-bit output digital word (B) a logical state according to the state of the data input (D_x) of the output module (OM) is assigned by means of the output module (OM), in such a way that if the data input (D_x) of the output module (OM) is put into active state by means of the first output (Q1) of the main MUTEX circuit (MM_x), then to the bit having index x (b_x) of the n-bit output digital word (B) a logical state one is assigned by means of the output module (OM), and otherwise, when the data input (D_x) of the output module (OM) is kept in the inactive state by means of the first output (Q1) of the main MUTEX circuit (MMx), to the bit having index x (b_x) of the n-bit output digital word (B) a logical state zero is assigned by means of the output module (OM).

2. The method according to claim 1, **characterized in that** the active state of the source signal (Sc_x), of the reference signal (Rf_x), of the first output (Q1) of the main MUTEX circuit (MM_x) and of the second output (Q2) of the main MUTEX circuit (MM_x) as well as of a first output (Q1) of the additional MUTEX circuit (MA_x) and of the second output (Q2) of the additional MUTEX circuit (MM_x) is a logical high state, whereas by means of the first gate (B1) and by means of the second gate (B2) a logical OR function is implemented.

3. The method according to claim 1, **characterized in that** the active state of the source signal (Sc_x), of the reference signal (Rf_x), of the first output (Q1) of the main MUTEX circuit (MM_x) and of the second output (Q2) of the main MUTEX circuit (MM_x) as well as of the first output (Q1) of the additional MUTEX circuit (MA_x) and of the second output (Q2) of the additional MUTEX circuit (MM_x) is a logical low state, whereas by means of the first gate (B1) and by means of the second gate (B2) a logical AND function is implemented.

4. The method according to claim 2 or 3, **characterized in that** the default logical states are assigned by means of the output module (OM) to selected bits of the n-bit output digital word (B) in such a way that to the bit having index x (b_x) of the n-bit output digital word (B) a logical state zero is assigned by means of the output module (OM), and to all possible less significant bits (b_{x-1}, ..., b_0) of the n-bit output digital word (B) logical states one are assigned by means of the output module (OM).

5. The method according to claim 2 or 3, **characterized in that** the default logical states are assigned by means of the output module (OM) to selected bits of the n-bit output digital word (B) in such a way that to the bit having index x (b_x) of the n-bit output digital word (B) a logical state one is assigned by means of the output module (OM), and to all possible less significant bits (b_{x-1}, ..., b_0) of the n-bit output digital word (B) logical states zero are assigned by means of the output module (OM).

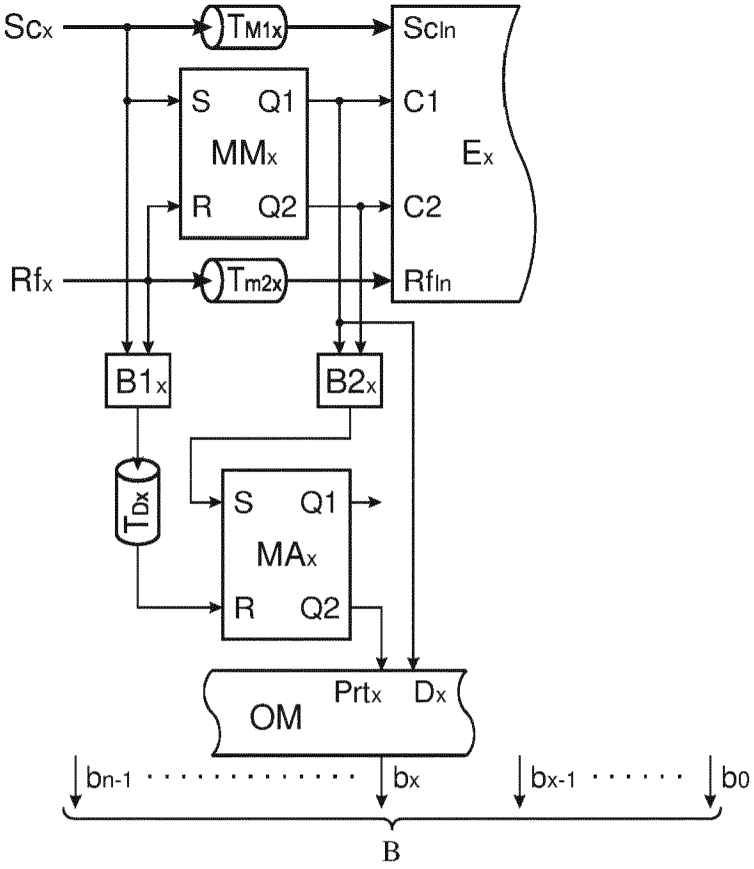

Fig. 1.

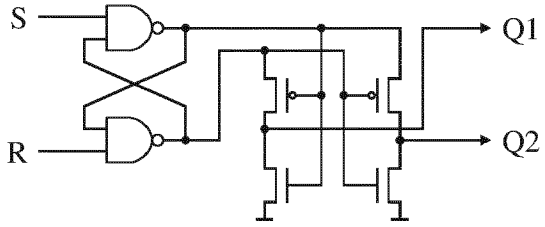

Fig. 2.

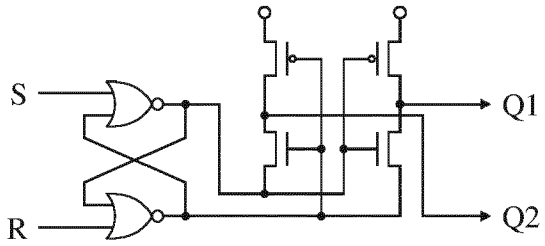

Fig. 3.

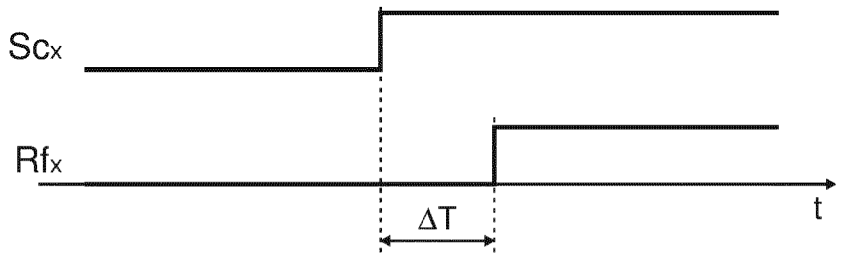

Fig. 4.

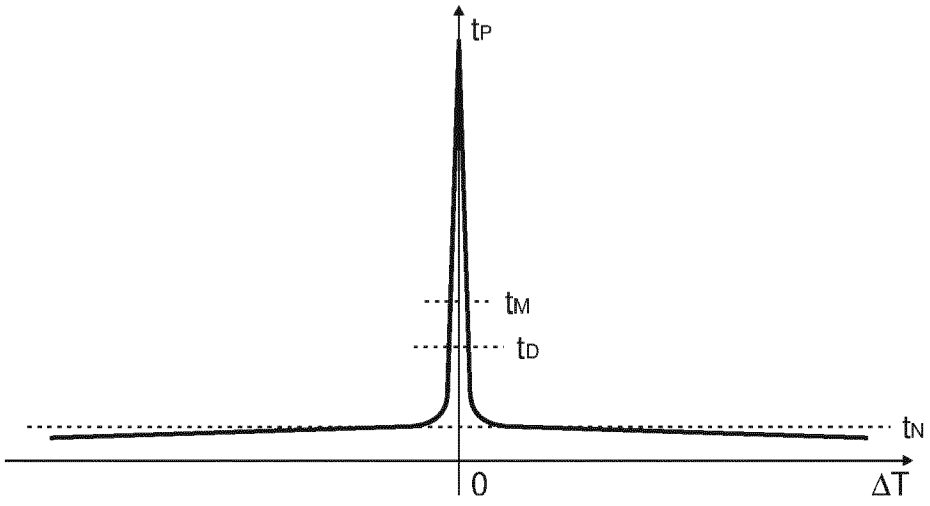

Fig. 5.

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EUROPEAN SEARCH REPORT

Application Number
EP 22 21 3666

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A	KOSCIELNIK DARIUSZ ET AL: "Optimized design of successive approximation time-to-digital converter with single set of delay lines", 2016 SECOND INTERNATIONAL CONFERENCE ON EVENT-BASED CONTROL, COMMUNICATION, AND SIGNAL PROCESSING (EBCCSP), IEEE, 13 June 2016 (2016-06-13), pages 1-8, XP032983233, DOI: 10.1109/EBCCSP.2016.7605284 [retrieved on 2016-10-20] * Paragraph II; Figures 4 and 8 * * Paragraph IV; Figures 11 ans 12 * * Paragraph V; Figure 15 * * Paragraph VI; Figure 20 * -----	1-5	INV. G04F10/00 H03M1/08
A	ABAS M A ET AL: "Embedded high-resolution delay measurement system using time amplification", 20070305, vol. 1, no. 2, 5 March 2007 (2007-03-05), pages 77-86, XP006028355, * Paragraph 2.2; Figure 3 * * Paragraphs 3.1 and 3.2; Figures 6, 7 and 13 * ----- -/--	1-5	TECHNICAL FIELDS SEARCHED (IPC) G04F H03M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	16 August 2023	Pirozzi, Giuseppe

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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A	SZYDUCZYNSKI J ET AL: "Behavioral Modelling and Optimization of a Cyclic Feedback-Based Successive Approximation TDC with Dynamic Delay Equalization", 2019 5TH INTERNATIONAL CONFERENCE ON EVENT-BASED CONTROL, COMMUNICATION, AND SIGNAL PROCESSING (EBCCSP), IEEE, 27 May 2019 (2019-05-27), pages 1-9, XP033617077, DOI: 10.1109/EBCCSP.2019.8836859 [retrieved on 2019-09-13] * the whole document *	1-5	TECHNICAL FIELDS SEARCHED (IPC)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
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