(19)

(12)





(11) EP 3 142 256 A1

EUROPEAN PATENT APPLICATION

(51) Int Cl.:

H03M 1/46 (2006.01)

- (43) Date of publication: 15.03.2017 Bulletin 2017/11
- (21) Application number: 15200947.8
- (22) Date of filing: 17.12.2015
- (84) Designated Contracting States: (71) Applicant: AKADEMIA GORNICZO-HUTNICZA AL AT BE BG CH CY CZ DE DK EE ES FI FR GB im. Stanislawa Staszica GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO 30-059 Krakow (PL) PL PT RO RS SE SI SK SM TR **Designated Extension States:** (72) Inventors: KOSCIELNIK, Dariusz BA ME 31-431 Krakow (PL) **Designated Validation States:** MA MD MISKOWICZ, Marek 31-636 Krakow (PL) (30) Priority: 14.09.2015 PL 41395815 14.09.2015 PL 41395915 (74) Representative: Kacperski, Andrzej Kancelaria Prawno-Patentowa ul. Kupa 3/9 31-057 Krakow (PL)

(54) METHOD AND APPARATUS FOR CONVERSION OF VALUE OF ANALOG SIGNAL TO COMPRESSED DIGITAL WORD

(57) Method for conversion of a value of an analog signal to a compressed digital word (CW) uses conversion of the analog signal to a linear digital word (LW) according to a successive approximation scheme. The process of conversion of the analog signal to the linear digital word (LW) is terminated by the compression module (CPM) when all bits of the compression word (CW) have been already evaluated.

Apparatus for conversion of a value of an analog signal to a compressed digital word a linear successive approximation analog-to-digital converter (SA-ADC).

The output of the linear digital word (LW) of this converter is connected to the input of the linear digital word (LW) of the compression module (CPM) comprising a section number register (RegS), while complete conversion signal output (End) of the compression module (CPM) is connected to a complete conversion signal input (End) of the linear analog-to-digital converter (SA-ADC), and a bit ready signal output (BitRdy) of the linear analog-to-digital converter (SA-ADC) is connected to a bit ready signal input (BitRdy) of the compression module (CPM).



Fig. 1.

Description

[0001] The subject of this invention is a method and an apparatus for a conversion of a value of an analog signal to a compressed digital word that can be applied in monitoring and control systems.

[0002] A conversion of a voltage value to a linear digital word using a successive approximation scheme is known from the article James McCreary, Paul R. Gray "A High-Speed, All-MOS Successive-Approximation Weighted Capacitor A/D Conversion Technique", IEEE International Solid-State Circuits Conference, February 12, 1975, pp. 38 - 39. The solution according to the aforementioned article uses a technique of charge redistribution among a number of m+1 capacitors, while m is a number of bits in the linear digital word. The capacitances of the capacitors are binary-weighted except the last capacitor whose capacitance is the same as the capacitance of the second-to-last capacitor. In the first stage of conversion, an input voltage is sampled which causes an accumulation of a charge portion in the capacitors that are connected in parallel to the input voltage, while the charge portion accumulated in the capacitors is proportional to a value of the input voltage. The accumulated charge portion is further redistributed among the capacitors by searching such a combination of capacitors connected in parallel that a voltage created on these capacitors by redistributed charge is as close to a given reference voltage as possible. At each conversion step, a capacitor which is connected to a set of capacitors has lower capacitance compared to a capacitor connected in a previous step. If a voltage created on the set of capacitors is higher than the reference voltage, the actually connected capacitor is kept connected to the set of capacitors in next steps, and a corresponding output bit is evaluated to one. Otherwise, the actually connected capacitor is disconnected from the set of capacitors, and a corresponding output bit is evaluated to zero.

[0003] A method of representation of a value of analog signal by a compressed digital word according to A law is known from the document ITU-T G.711 "Pulse code modulation of voice frequencies". A full scale input range for positive signal values and a full scale input range for negative signal values of the analog-to-digital converter are split into eight unequal sections. The sections no. 7 correspond to upper halves of the full scale input range for absolute negative and positive values of the analogto-digital converter. Each section of a lower index corresponds to upper halves of remaining parts of full scale input range except the section no. 0 whose range is the same as the range of the section no. 1. Each section is split into 16 quantization steps. The most significant bit of a compressed digital word according to A law represents a sign of a value of input signal. The next 3 bits represent an index of a section to which the value of input signal corresponds. The 4 least significant bits of the compressed digital word according to A law represents an index of a quantization step to which the value of input

signal corresponds.

[0004] A method for conversion of a voltage value to a compressed digital word according to successive approximation scheme is known from the article Eberhard Pfrenger, Peter Picard and Frithjof von Sichart "A Companding D/A Converter for a Dual-Channel PCM CO-DEC", IEEE International Solid-State Circuits Conference, February 16, 1978, pp. 186 - 187. Bits of the n-bit compressed digital word are evaluated successively by

¹⁰ the use of a successive approximation register (SAR) starting from the most significant bit. In each step, a tested bit is set to one and provided via an expander to an input of m-bit linear digital-to-analog converter in order to create an approximation of the converted value of the analog input signal. If the created approximation is higher

¹⁵ analog input signal. If the created approximation is higher than the value of analog input signal, then the corresponding output bit is set to zero. Otherwise, output bit is set to one. The number of conversion steps is not lower than n+1 and independent of the value of the analog input
 ²⁰ signal.

[0005] An apparatus for conversion of a voltage value to a linear digital word according to successive approximation scheme is known from the article James Mc-Creary, Paul R. Gray "A High-Speed, All-MOS Succes-25 sive-Approximation Weighted Capacitor A/D Conversion Technique", Proceedings of IEEE International Solid-State Circuits Conference, February 1975, pp. 38-39. The aforementioned apparatus comprises a successive approximation capacitor array whose one input is con-30 nected to a source of converted input voltage, whereas the other input is connected to a source of the reference voltage while its output is connected to a control module through a comparator. The control module is equipped with a digital output and an input of the clock signal that 35 clocks a conversion process. Two control outputs of the control module are connected to the comparator, and the other control outputs of the control module are connected to the successive approximation capacitor array.

[0006] The successive approximation capacitor array comprises a number of n capacitors of binary-weighted capacitances and an additional capacitor while the first plate of each capacitor in the array is connected to the first common rail, and the capacitance of the additional capacitor equals the capacitance of the smallest capac-

⁴⁵ itor in the array. The other plates of the capacitors in the array are connected to the other common rail through the change-over switches whose other stationary contacts are connected to the ground of the circuit. The first common rail is connected to the non-inverting input of the comparator, and the second common rail is connect-

ed through another switch to the source of the input voltage or to the source of the reference voltage, while the inverting input of the comparator is connected to the ground of the circuit.

⁵⁵ **[0007]** Method and apparatus for conversion of a time interval to a digital word is known from the patent document US 9,063,518. The apparatus comprises an array of capacitors whose control inputs are connected to a set

10

of control outputs of a control module. The control module is equipped with a digital output, a complete conversion signal output, a trigger input and two control inputs. The first control input is connected to the output of the first comparator whose inputs are connected to one pair of outputs of the array of capacitors, and the other control input of the control module is connected to the output of the second comparator whose inputs are connected to the other pair of outputs of the array. Besides, the source of auxiliary voltage together with the source of the reference voltage, the sampling capacitor, and two controlled current sources are connected to the set of capacitors while control inputs of both current sources are connected to control outputs of the control module.

[0008] An apparatus for conversion of a voltage value to a compressed digital word according to successive approximation scheme is known from the article Eberhard Pfrenger, Peter Picard and Frithjof von Sichart "A Companding D/A Converter for a Dual-Channel PCM CODEC", IEEE International Solid-State Circuits Conference, February 16, 1978, pp. 186 - 187. The aforementioned apparatus comprises a comparator whose noninverting input is used to provide an analog input signal. A comparator output is connected to an input of successive approximation register SAR comprising n-bit digital output, which is used to output a compressed digital word. This output is connected to n-bit input of an expander whose m-bit output of a linear digital-to-analog converter. A converter output is connected to an inverting input of the comparator.

[0009] Method for conversion of a value of an analog signal to a compressed digital word, according to the invention, uses a conversion of the value of the analog signal to a linear digital word by means of a successive approximation scheme. A number of bits of the linear digital word is not lower than m, and at the same time, the number of bits of the linear digital word is higher than a number of bits of a compressed digital word, which is not lower than n. The number of bits of the compressed digital word is not lower than n, whereas bits of the linear digital word are evaluated by the use of a linear analog-to-digital converter and are provided to a linear digital input.

[0010] The essence of the method is that the conversion of the value of the analog signal to the linear digital word is terminated by the use of a compression module when all bits of the compression word are already evaluated. A compression starts when the compression module detects an active state on a compression trigger input, and then a number equal to a difference between numbers m and v is written to a section number register in the compression module, while v is an arbitrarily chosen natural number smaller than n. After detection, on the basis of a bit ready signal, that a new output bit in the linear digital word has been evaluated by the linear analog-to-digital converter, a content of the section number register is decreased by one if a state of the new output bit equals zero. The content of the section number register

ister is not decreased if a state of the new output bit equals one, or if the content of the section number register has been already reduced to zero, and then, in both cases, the evaluation of next v bits of the linear digital word by the linear analog-to-digital converter is awaited, and a number of occurrences of bit ready signal is counted. Afterwards, a complete conversion signal is generated

by the compression module which terminates the conversion of the analog signal to the linear digital word, and introduces the linear analog-to-digital converter to a stand by state, while the states of v bits of the linear digital

word evaluated recently are assigned respectively to the least significant v bites of the compressed digital word, and the content of the section number register is written

¹⁵ to the more significant bites of the compressed digital word.

[0011] It is advantageous if the analog signal is unipolar, the compressed digital word contains a number of n=s+v bits, and a process of decreasing of the content
of the section number register is started as soon as the most significant bit in the linear digital word, having a number of m bits, is evaluated by the linear analog-to-

digital converter.
[0012] It is advantageous if the analog signal is bipolar,
the compression word contains a number of n+1=s+v+1 bits, and a process of decreasing of the content of the section number register is started as soon as a bit following the most significant bit in the linear digital word, having a number of m+1 bits, is evaluated by the linear analog-to-digital converter, while a state of the most significant bit in the linear digital word representing a sign of an analog signal value according to a sign-magnitude format is by the use of the compression module assigned to the most significant bit of the compressed digital word shaving the number of m+1 bits.

³⁵ having the number of m+1 bits.
 [0013] Apparatus, according to invention, comprises a successive approximation analog-to-digital converter. A linear digital word output having a number of bits not lower than m is connected to a linear digital input of a compression module comprising a compressed digital output

pression module comprising a compressed digital output having a number of bits not lower than n. The number of bits of the linear digital input is not higher than the number of bits of a compressed digital word.

The essence of the method is that a compression module
comprises a section number register. A complete conversion signal output of the compression module is connected to a complete conversion signal input of the linear analog-to-digital converter. A bit ready signal output of the linear analog-to-digital converter is connected to a
bit ready signal input of the compression module.

[0014] It is advantageous if a compression trigger input of the compression module is connected to a conversion trigger input of the linear analog-to-digital converter.

 [0015] It is advantageous if the compression trigger
 ⁵⁵ input of the compression module is connected to an analog input of the linear analog-to-digital converter.

[0016] It is advantageous if the linear analog-to-digital converter is a synchronous device, and a bit ready signal

output of the linear analog-to-digital converter comprises a single line transmitting a signal that provides timing for the linear analog-to-digital converter operation.

[0017] It is advantageous if the linear analog-to-digital converter is a known asynchronous device comprising two comparators, and a bit ready signal output of the linear analog-to-digital converter contains two lines that transmit output signals of both comparators.

[0018] It is advantageous if the linear analog-to-digital converter is a converter of a unipolar input signal comprising a linear output having a number of m bits, while the compression module contains an output of the compressed digital word having a number of n bits.

[0019] It is advantageous if the linear analog-to-digital converter is a converter of a bipolar input signal comprising a linear output having a number of m+1 bits representing a sign-magnitude format, while the compression module contains an output of the compressed digital word having a number of n+1 bits.

[0020] The solution according to the invention is characterized by a reduction of the number of steps of the linear analog-to-digital conversion required for evaluation of bits of the compressed digital word. Therefore, both conversion time and energy needed to convert an analog signal value to the compressed digital word are decreased.

[0021] The solution according to the invention is presented in the following figures:

Fig. 1 illustrates the block diagram of the apparatus, in which the compression trigger input TrgCP of the compression module CPM is connected to the conversion trigger input TrgADC of the synchronous linear analog-to-digital converter SA-ADC.

Fig. 2 illustrates the block diagram of the apparatus, in which the linear analog-to-digital converter SA-ADC is a known asynchronous device, and a bit ready signal output BitRdy contains two lines.

Fig. 3 illustrates a format of the linear digital word LW and the compressed digital word CW for conversion of unipolar signal.

Fig. 4 illustrates a format of the linear digital word LW according to a sign-magnitude representation and the compressed digital word CW for conversion of bipolar signal.

[0022] Method for conversion of a value of an analog signal to a compressed digital word, according to the invention, adopts a conversion of a unipolar analog signal to a linear digital word using successive approximation scheme. Bits of the linear digital word LW, having a number of m=11 bits are evaluated successively using the linear analog-to-digital converter SA-ADC, and are provided to the linear digital input LW of a compression module CPM.

[0023] The conversion of a value of the analog signal to the linear digital word LW is terminated by the use of the compression module CPM as soon as all the bits of the compressed digital word CW, having a number of bits equal to 7, are evaluated. The compression process is started when an active state on a compression trigger

input TrgCP is detected by the compression module CPM. Then, a number 7 equal to a difference between the numbers m=11 and v=4 is written to a section number

¹⁰ register (RegS) in the compression module CPM, while v=4 is chosen arbitrarily. After detection, on the basis of a bit ready signal BitRdy, that a new output bit in the linear digital word LW has been evaluated by a linear analogto-digital converter SA-ADC, a content of the section

¹⁵ number register RegS is decreased by one if a state of the new output bit has been evaluated to zero. The reduction of the content of the section number register RegS is started as soon as the most significant bit in the linear digital word LW is evaluated on the output the linear

20 analog-to-digital converter SA-ADC. The content of the section number register RegS is not reduced if a state of the new output bit in the linear digital word LW has been evaluated to one, or if the content of the section number register RegS has been already reduced to zero. Then,

in both cases, the evaluation of the next v bits of the linear digital word LW by the linear analog-to-digital converter SA-ADC is awaited, while a number v is equal to 4, and a number of occurrences of bit ready signal BitRdy up to 4 has been counted. Afterwards, a complete conversion signal End is generated by the compression module CPM, which terminates the conversion of the analog signal value to the linear digital word LW and introduces the linear analog-to-digital converter SA-ADC to a stand by state. The states of v=4 bits of the linear digital word LW
evaluated recently are assigned respectively to the least

significant v=4 bites of the compressed digital word CW. The content of the section number register RegS is written to a number of s of more significant bites of the compressed digital word CW, while s is equal to 3.

40 [0024] In another variant of the method for conversion of a value of the analog signal to the compressed digital word, according to the invention, adopts a conversion of a bipolar analog signal to the linear digital word using successive approximation scheme. A number of m+1 bits 45 of the linear digital word I W equals 12 and a number of 46 of the linear digital word I W equals 12 and a number of 47 of the linear digital word I W equals 12 and a number of 48 of the linear digital word I W equals 12 and a number of 49 of the linear digital word I W equals 12 and a number of 49 of the linear digital word I W equals 12 and a number of

of the linear digital word LW equals 12, and a number of n+1 bits of the compression word CW equals 8. [0025] This variant of the method differs from the previous variant in that a process of reduction of the content of the section number register RegS is started as soon as a bit following the most significant bit in the linear digital word LW has been evaluated by the linear analog-to-digital converter SA-ADC. A state of the most significant bit in the linear digital word LW representing a sign of an analog signal value Sg according to a sign-magnitude format is by the use of the compression module CPM

assigned to the most significant bit of the compressed digital word CW (Fig. 4).

[0026] The apparatus for conversion of a value of the

50

55

analog signal to the compressed digital word in the first embodiment, according to the invention, comprises the 11-bit synchronous unipolar linear successive approximation analog-to-digital converter SA-ADC (Fig. 1). A linear digital word LW output of the linear analog-to-digital converter SA-ADC, having a number of bits equal to 11, is connected to a linear digital word LW input of a compression module CPM comprising a section number register RegS and a compressed digital word CW output, having a number of bits equal to 7, a and complete conversion signal output End, connected to a complete conversion signal input End of the linear analog-to-digital converter SA-ADC. A bit ready signal output BitRdy of the linear analog-to-digital converter SA-ADC comprising a single line transmitting a signal that provides timing for the linear analog-to-digital converter SA-ADC operation is connected to a bit ready signal input BitRdy of the compression module CPM. A compression trigger input TrgCP of the compression module CPM is connected to a conversion trigger input TrgADC of the linear analogto-digital converter SA-ADC.

[0027] In the second embodiment, the apparatus comprises a known 11-bit synchronous unipolar linear successive approximation analog-to-digital converter SA-ADC comprising a set of capacitors A connected to a control module CM by the use of lines transmitting control signals Ctr (fig. 2). A first comparator K1 and a second comparator K2 are connected to the set of capacitors A. Outputs of both comparators are connected respectively to a first input In1 and to a second input In2 of the control module CM. An output of the linear digital word LW of the control module CM, having a number of bits m equal to 11, is connected to an input of the linear digital word of the compression module CPM comprising a section number register RegS, and an output of the compressed digital word CW having a number of bits n equal to 7, and a complete conversion signal output End of the control module CM. A bit ready signal output BitRdy of the linear analog-to-digital converter SA-ADC, comprising two lines transmitting output signals both of the first comparator K1 and of the second comparator K2, is connected to a bit ready signal input BitRdy of the compression module CPM. A compression trigger input TrgCP of the compression module CPM is connected to an analog input InADC of the control module CM, which is the input for conversion of time intervals.

[0028] In the third embodiment, the apparatus differs from the first embodiment in that the apparatus comprises a 12-bit synchronous bipolar linear analog-to-digital converter SA-ADC, whose output of the linear digital word LW, having a number of bits m+1=12 is connected to the input of the linear digital word of the compression module CPM (fig. 1). The compression module CPM comprises the output of the compressed digital word CW having a number of bits n+1=8.

[0029] The conversion of a value of the analog signal to the compressed digital word In the first embodiment is realized as follows (Fig. 1). As soon as an active state

on a compression trigger input TrgCP is detected by the compression module CPM, a number m-v=7 is written to a section number register RegS in the compression module CPM. At the same time, an active state of the conversion trigger input TrgADC by the linear analog-to-digital converter SA-ADC, the conversion of a unipolar value of an analog signal provided to the analog input InADC to the linear digital word LW, having a number of bits equal to 11, according to a known successive approxi-

¹⁰ mation scheme, is started. The states of bits of the linear digital word LW are successively evaluated in a known way by the linear analog-to-digital converter SA-ADC, and at the same time provided to the input of the linear digital word of the compression module CPM.

¹⁵ [0030] The linear analog-to-digital converter SA-ADC by the use of the bit ready signal BitRdy signalizes to the compression module CPM that a new output bit in the linear digital word LW has been evaluated. As soon as the compression module CPM, on the basis of the bit ready signal BitRdy, detects that a new output bit in the linear digital word LW by the linear analog-to-digital converter SA-ADC has been evaluated, the content of the section number register RegS is decreased by one if a state of a new output bit in the linear digital word LW has

25 been evaluated to zero, and the cycle of evaluation and the analysis of next bits are repeated. The compression module CPM terminates a process of decreasing the content of the section number register RegS if a state of a new output bit in the linear digital word LW has been 30 evaluated to one, or if the content of the section number register actually RegS has been already reduced to zero. [0031] Then, in both cases, the evaluation of the next v bits of the linear digital word LW by the linear analogto-digital converter SA-ADC is awaited, and a number of 35 v occurrences of the bit ready signal BitRdy is counted, while v equals 4. Afterwards, a complete conversion signal End is generated by the compression module CPM,

which terminates the conversion of the analog signal to the linear digital word LW, and introduces the linear analog-to-digital converter SA-ADC to a stand by state. The states of v bits of the linear digital word LW evaluated recently are assigned by the compression module CPM respectively to the least significant v bites of the compressed word CW, while v equals 4 (Fig. 3). The content

45 of the section number register RegS is written by the compression module CPM to the more significant s bites of the compressed word CW, while s equals 3 (Fig. 3). [0032] The conversion of a value of an analog signal to a compressed digital word in the second embodiment 50 (Fig. 2) is realized as follows. As soon as an active state on a compression trigger input TrgCP is detected by the compression module CPM, a number equal to 7 which is a difference between numbers m and v is written to a section number register RegS in the compression mod-55 ule CPM. At the same time, when a beginning of a time interval which is signalled at an analog input InADC, the linear analog-to-digital converter SA-ADC starts the conversion of the time interval provided to the analog input InADC to the linear digital word LW, having a number of bits equal to 11, according to a known successive approximation scheme. The values of bits of the linear digital word LW are successively evaluated in a known way by the linear analog-to-digital converter SA-ADC, and at the same time provided to the input of the linear digital word of the compression module CPM.

[0033] The linear analog-to-digital converter SA-ADC terminates the evaluation of the output bits when a short active state is generated on the output of the first comparator K1, or on the output of the second comparator K2. The states of the outputs of both comparators are transmitted by the use of two lines of the bit ready signal output BitRdy of the compression module CPM.

[0034] As soon as the compression module CPM, on the basis of the bit ready signal BitRdy, detects that a new output bit in the linear digital word LW by the linear analog-to-digital converter SA-ADC has been evaluated, the content of the section number register RegS is decreased by one if a state of the new output bit in the linear digital word LW has been evaluated to zero, and the cycle of evaluation and the analysis of next bits is repeated. The compression module CPM terminates a process of decreasing the content of the section number register RegS if a state of a new output bit in the linear digital word LW has been evaluated to one, or if the content of the section number register actually RegS has been already reduced to zero.

[0035] Then, in both cases, the conversion of the value 30 of the analog signal to the compressed digital word is continued in the same way as in the first embodiment. [0036] The conversion of a value of an analog signal to a compressed digital word in the third embodiment differs from the conversion in the first embodiment in that the compression module CPM starts the process of de-35 creasing of the content of the section number register RegS as soon as a bit following the most significant bit in the linear digital word LW. The state of the most significant bit in the linear digital word LW representing a 40 sign of an analog signal value Sg according to a signmagnitude format is by the use of the compression module CPM assigned to the most significant bit of the compressed word CW (Fig. 4).

Acronims

[0037]

SA-ADC	linear analog-to-digital converter	
CPM	compression module	50
InADC	analog input	
RegS	section number register	
LW	linear digital word	
CW	compressed digital word	
End	complete conversion signal	55
BitRdy	bit ready signal	
TrgADC	conversion trigger input	
TrgCP	compression trigger input	

	Sg	sign of an analog signal value
	А	set of capacitors
	СМ	control module
	K1	first comparator
5	K2	second comparator
	ln1	first input of control module
	In2	second input of control module

10 Claims

15

20

25

1. Method for conversion of a value of an analog signal to a compressed digital word using a conversion of the analog signal to a linear digital word according to a successive approximation scheme, while a number of bits of the linear digital word is not lower than m, and at the same time, the number of bits of the linear digital word is higher than a number of bits of a compressed digital word, and the number of bits of the compressed digital word is not lower than n, whereas the bits of the linear digital word are already evaluated by the use of a linear analog-to-digital converter and provided to a linear digital input characterized in that the conversion of a value of the analog signal to the linear digital word (LW) is terminated by the use of a compression module (CPM) when all bits of the compression word (CW) are already evaluated, while a compression starts when the compression module (CPM) detects an active state on a compression trigger input (TrgCP), and then a number equal to a difference between numbers m and v is written to a section number register (RegS) in the compression module (CPM), while v is an arbitrarily chosen natural number smaller than n, and after detection, on the basis of a bit ready signal (BitRdy), that a new output bit in the linear digital word (LW) has been evaluated by the linear analog-to-digital converter (SA-ADC), a content of the section number register (RegS) is decreased by one if a state of the new output bit in the linear digital word (LW) has been evaluated to zero, while the content of the section number register (RegS) is not decreased if a state of the new output bit in the linear digital word (LW) has been evaluated to one, or if the content of the section number register (RegS) has been already reduced to zero, and then, in both cases, the evaluation of next v bits of the linear digital word (LW) by the linear analog-to-digital converter (SA-ADC) is awaited, and a number of v occurrences of a bit ready signal (BitRdy) is counted, and afterwards, a complete conversion signal (End) is generated by the compression module (CPM), which terminates the conversion of the analog signal to the linear digital word (LW), and introduces the linear analog-to-digital converter (SA-ADC) to a stand by state, while the states of v bits of the linear digital word (LW) evaluated recently are assigned by the compression module CPM respectively to the least

45

10

15

20

25

- Method as claimed in claim 1 characterized in that 2. the analog signal is unipolar, the compression word (CW) contains a number of n=s+v bits, and a process of decreasing of the content of the section number register (RegS) is started as soon as the most significant bit in the linear digital word (LW), having a number of m bits, is evaluated by the linear analogto-digital converter (SA-ADC).
- 3. Method as claimed in claim 1 characterized in that the analog signal is bipolar, the compression word (CW) contains a number of n+1=s+v+1 bits, and a process of decreasing of the content of the section number register (RegS) is started as soon as a bit following the most significant bit in the linear digital word (LW), having a number of m+1 bits, is evaluated by the linear analog-to-digital converter (SA-ADC), while a state of the most significant bit in the linear digital word (LW) representing a sign of an analog signal value (Sg) according to a sign-magnitude format is by the use of the compression module (CPM) assigned to the most significant bit of the compressed word (CW) having the number of m+1 bits.
- 4. Apparatus for conversion of a value of an analog 30 signal to a compressed digital word using a conversion of a value of an analog signal to a linear digital word according to a successive approximation scheme whose linear digital word output having a number of bits not lower than m is connected to a 35 linear digital word input of a compression module comprising a compressed digital output having a number of bits not lower than n, while the number of bits of the linear digital word input is not higher than 40 the number of bits of the compressed digital word characterized in that the compression module (CPM) comprises a section number register (RegS), while a complete conversion signal output (End) of the compression module (CPM) is connected to a complete conversion signal input (End) of the linear analog-to-digital converter (SA-ADC), and a bit ready signal output (BitRdy) of the linear analog-todigital converter (SA-ADC) is connected to a bit ready signal input (BitRdy) of the compression module (CPM).
- 5. Apparatus as claimed in claim 4 characterized in that a compression trigger input (TrgCP) of the compression module (CPM) is connected to a conversion trigger input (TrgADC) of the linear analog-to-digital 55 converter (SA-ADC).
- 6. Apparatus as claimed in claim 4 characterized in

that the compression trigger input (TrgCP) of the compression module (CPM) is connected to an analog input (InADC) of the linear analog-to-digital converter (SA-ADC).

- 7. Apparatus as claimed in claim 5 or claim 6 characterized in that the linear analog-to-digital converter (SA-ADC) is a synchronous device, and a bit ready signal output (BitRdy) of the linear analog-to-digital converter (SA-ADC) comprises a single line transmitting a signal that provides timing for the linear analog-to-digital converter (SA-ADC) operation.
- Apparatus as claimed in claim 5 or claim 6 charac-8. terized in that the linear analog-to-digital converter (SA-ADC) is a known asynchronous device comprising two comparators, and a bit ready signal output (BitRdy) of the linear analog-to-digital converter (SA-ADC) contains two lines that transmit output signals of both comparators.
- 9. Apparatus as claimed in claim 7 or claim 8 characterized in that the linear analog-to-digital converter (SA-ADC) is a converter of a unipolar input signal comprising a linear output (LW) having a number of m bits, while the compression module (CPM) contains an output of the compressed word (CW) having a number of n bits.
- 10. Apparatus as claimed in claim 7 or claim 8 characterized in that the linear analog-to-digital converter (SA-ADC) is a converter of a bipolar input signal comprising a linear output (LW) having a number of m+1 bits representing a sign-magnitude format, while the compression module (CPM) contains an output of the compressed word (CW) having a number of n+1 bits.

7

45

50



Fig. 1.



Fig. 2.



Fig. 3.



Fig. 4.





EUROPEAN SEARCH REPORT

Application Number EP 15 20 0947

	DOCUMENTS CONSIDERED TO BE RELEVANT				
	Category	Citation of document with in of relevant passa	dication, where appropriate, ages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
10 15	X	LAMPINEN H ET AL: Successive-Approxim CONFERENCE PROCEEDI INTERNATIONAL SYMPO SYSTEMS (ISCAS) : M INTERNATIONAL CONFE JAPAN. IEEE SERVICE	"Novel ation Algorithms", NGS / IEEE SIUM ON CIRCUITS AND AY 23 - 26, 2005, RENCE CENTER, KOBE, CENTER, PISCATAWAY.	1-10	INV. H03M1/46
20 25		NJ, 23 May 2005 (2005-0 XP010815509, DOI: 10.1109/ISCAS. ISBN: 978-0-7803-88 * abstract * * Section I * * Section I * * Section II * * Section III * * figures 1,2b *	5-23), pages 188-191, 2005.1464556 34-5		
30	Х	LAMPINEN H ET AL: compressing A/D con PROCEEDINGS OF 1997 SYMPOSIUM ON CIRCUI	"A new dual-mode data verter", IEEE INTERNATIONAL TS AND SYSTEMS, 1997.	1-10	TECHNICAL FIELDS SEARCHED (IPC)
35		ISCAS '9/., HONG KO YORK, NY, USA,IEEE, vol. 1, 9 June 1997 429-432, XP01023606 DOI: 10.1109/ISCAS. ISBN: 978-0-7803-35 * abstract *	NG 9-12 JUNE 1997, NEW US, (1997-06-09), pages 7, 1997.608759 83-7		нөзм
40		* Section I * * Section II * * Section III * * figure 1b * * tables 1,2 *			
45					
1		The present search report has b	been drawn up for all claims		Evaminar
50 fg				Doc	ha Daniol
P04C	пе надие		10 January 2017	kocna, Daniel	
255 (1) 28 00 28 00 20 20 20 20 20 20 20 20 20 20 20 20	CATEGORY OF CITED DOCUMENTS T : theory or principle underlying the invention X : particularly relevant if taken alone E : earlier patent document, but published on, or after the filing date Y : particularly relevant if combined with another D : document of the same category A : technological background Category			nvention hed on, or	
PO FC	C P : intermediate document document document				, conesponding



EP 3 142 256 A1

EUROPEAN SEARCH REPORT

Application Number EP 15 20 0947

	DOCUMENTS CONSIDERED TO BE RELEVANT				
	Category	Citation of document with ir of relevant passa	ndication, where appropriate, ages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
10	Т	Anonymous: "G.711"	9		
15		27 July 2015 (2015- Retrieved from the URL:https://en.wiki itle=G.711&oldid=67 [retrieved on 2017-	07-27), XP055335925, Internet: pedia.org/w/index.php?t 3380431 01-17] 		
20					
25					
30					TECHNICAL FIELDS SEARCHED (IPC)
35					
40					
45					
1		The present search report has b	been drawn up for all claims		
50 fo		The Hague	Date of completion of the search	Roc	ha. Daniel
3.82 (P040	C,	ATEGORY OF CITED DOCUMENTS	T : theory or principle E : earlier patent doo	underlying the ir iment, but publis	ivention hed on, or
55 855 WHO J Od	X : particularly relevant if taken alone after the filing date Y : particularly relevant if combined with another D : document cited in the application document of the same category L : document cited for other reasons A : technological background				corresponding

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

• US 9063518 B [0007]

Non-patent literature cited in the description

- JAMES MCCREARY; PAUL R. GRAY. A High-Speed, All-MOS Successive-Approximation Weighted Capacitor A/D Conversion Technique. *IEEE International Solid-State Circuits Conference*, 12 February 1975, 38-39 [0002]
- EBERHARD PFRENGER; PETER PICARD; FRITHJOF VON SICHART. A Companding D/A Converter for a Dual-Channel PCM CODEC. *IEEE International Solid-State Circuits Conference*, 16 February 1978, 186-187 [0004] [0008]
- JAMES MCCREARY; PAUL R. GRAY. A High-Speed, All-MOS Successive-Approximation Weighted Capacitor A/D Conversion Technique. Proceedings of IEEE International Solid-State Circuits Conference, February 1975, 38-39 [0005]