(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 3 141 968 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
31.03.2021 Bulletin 2021/13

(51) Int Cl.:
G04F 10/00 *(2006.01)*

(21) Application number: **15200980.9**

(22) Date of filing: **17.12.2015**

(54) **METHOD AND APPARATUS FOR CONVERSION OF TIME INTERVAL TO DIGITAL WORD USING SUCCESSIVE APPROXIMATION SCHEME**

VERFAHREN UND VORRICHTUNG ZUR UMWANDLUNG EINES ZEITINTERVALLS IN DIGITALES WORT DURCH SCHEMA DER SCHRITTWEISEN ANNÄHERUNG

PROCÉDÉ ET APPAREIL DE CONVERSION D'INTERVALLE DE TEMPS EN MOT NUMÉRIQUE UTILISANT UN SCHÉMA D'APPROXIMATIONS SUCCESSIVES

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **14.09.2015 PL 41396015**
14.09.2015 PL 41396415

(43) Date of publication of application:
15.03.2017 Bulletin 2017/11

(73) Proprietor: **AKADEMIA GORNICZO-HUTNICZA im. Stanislawa Staszica**
30-059 Krakow (PL)

(72) Inventors:
- **KOSCIELNIK, Dariusz**
  31-431 Krakow (PL)
- **MISKOWICZ, Marek**
  31-636 Krakow (PL)

(74) Representative: **Kacperski, Andrzej**
Kancelaria Prawno-Patentowa
ul. Kupa 3/9
31-057 Krakow (PL)

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EP 3 141 968 B1

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] The subject of this invention is a method and an apparatus for conversion of a time interval to a digital word using a successive approximation scheme that can be applied in monitoring and control systems.

[0002] A method for conversion of a time interval to a digital word known from a patent description US 9,063,518 (WO2011/152744) consists of two stages.

[0003] In the first stage, a time interval is translated to a portion of electric charge through charging a sampling capacitor by a current source during the input time interval. The portion of electric charge is directly proportional to the time interval. After detection of an end of the time interval, the second stage of conversion starts. During the second stage of conversion, the portion of electric charge is converted to the digital word by its redistribution from the sampling capacitor to a set of capacitors of binary-weighted capacitances. Each capacitor corresponds to a bit in output digital word.

[0004] In each step of the second stage of conversion, the redistribution is realized by charge transfer between two capacitors. A capacitor that is actually a source of charge is called a current source capacitor. A capacitor that actually collects charge is called a current destination capacitor. The current destination capacitor has always lower capacitance than the current source capacitor. Moving the charge results in growing the voltage on the current destination capacitor and at the same time in falling the voltage on the current source capacitor. If the voltage on the current destination capacitor reaches the reference voltage before the voltage on the current source capacitor falls to zero, then, in the next conversion step, the charge transfer is continued to a new destination capacitor whose capacitance is twice lower than a capacitance of the current destination capacitor. If the voltage on the current source capacitor falls to zero before the current destination capacitor reaches the reference voltage, then, in the next conversion step, the current destination capacitor becomes a new source capacitor, and a new destination capacitor has a capacitance twice lower than a capacitance of the current destination capacitor. If a voltage on a particular capacitor equals the reference voltage, then a value one is assigned to a bit in the output digital word corresponding to this capacitor, and a value zero is assigned to other bits.

[0005] An apparatus for conversion of a time interval to a digital word known from the patent description US 9,063,518 (WO2011/152744) comprises a sampling capacitor and a set of binary-weighted capacitances. The bottom plate of each capacitor is connected through a change-over switch to the ground of the circuit, or to a source of auxiliary voltage, while a value of auxiliary voltage is higher enough than a value of a reference voltage. A non-inverting input of a first comparator is also connected to the source of auxiliary voltage. The first comparator is used to detect that a source capacitor is completely discharged. The inverting input of the first comparator is connected to a source rail. A non-inverting input of a second comparator is connected to the source of reference voltage, and an inverting input of the second comparator is connected to a destination rail. The second comparator is used to detect that a voltage on a destination capacitor reaches the reference voltage. The destination rail is connected through an on-off switch to the ground of the circuit and to an output of a current source whose input is connected through a change-over switch to the source rail or to a source of supply voltage. A top plate of each capacitor is connected through a source on-off switch to the source rail, and a destination on-off switch to the destination rail. Control inputs of the change-over switches and on-off switches are connected to relevant control outputs of a control module. A destination on-off switch corresponding to a given capacitor is controlled by the same control output of the control module, while a source on-off switch is controlled by another control output of the control module. Outputs of both comparators and a time input are also connected to the control module. Besides, the control module comprises a digital output and a complete conversion output.

[0006] A method for conversion of a time interval to a digital word using a successive approximation scheme consists in a detection of a beginning and of an end of the time interval by the use of a control module and in assignment of a corresponding binary value represented by n-bit output digital word to the time interval by the use of the control module.

[0007] The present invention relates to a method for conversion of a time interval to a digital word using a successive approximation scheme according to claim 1 and to an apparatus for conversion of a time interval to a digital word using a successive approximation scheme according to claim 5.

[0008] The essence of the method, according to the invention, consists in that the time interval is mapped to a difference of a length of a reference time and a length of a signal time. The reference time is generated from an instant when the beginning of the time interval is detected by the use the control module, and the signal time is generated from an instant when the end the time interval is detected by the use the control module. The generation of the reference time and the signal time is terminated at the same instant.

[0009] According to the invention the generation of the reference time is realized by charging a capacitor using a reference current source, while this capacitor is selected by the use of the control module from a set of capacitors that comprise capacitors, such that a capacitance of a capacitor of a given index is twice as high as a capacitance of a capacitor of the previous index. A capacitor of the highest capacitance in the set of capacitors is selected first. A selected capacitor is charged as long as the reference voltage increasing on the selected capacitor and compared to the threshold voltage by the use of the reference comparator reaches the threshold voltage. Then, a next capacitor in the set of capacitors is started to be charged while this capacitor has the highest capacitance among the capacitors that have not

been charged yet. The reference voltage increasing on the capacitor being charged is compared to the threshold voltage by the use of the reference comparator, and the cycle is repeated to the end of generation of both time intervals.

[0010] The generation of the signal time is realized by charging a capacitor by the use of the signal current source, while this capacitor selected by the use of the control module from a set of capacitors has the highest capacitance among the capacitors that have not been charged yet. The selected capacitor is charged as long as the signal voltage increasing on this capacitor and compared to the threshold voltage by the use of the signal comparator equals the threshold voltage. Then, a next capacitor in the set of capacitors is started to be charged by the use of the signal current source while this capacitor is selected in the same way and the cycle is repeated to the end of generation of both time intervals.

[0011] The generation of the reference time, and the generation of the signal time are terminated during the time when the capacitor of the lowest capacitance in the set of capacitors is charged, and when the reference voltage increasing on a capacitor charged by the use of the reference current source, or when the signal voltage increasing on a capacitor charged by the use of the signal current source reaches the threshold voltage.

[0012] It is advantageous if intensity of the reference current source is lower than intensity of the signal current source during the time interval, and intensity of the reference current source is increased by the use of the control module to intensity of the signal current source at the instant when generation of the time interval is terminated by the use of the control module.

[0013] It is advantageous if a value representing n-bit output digital word being a conversion result is evaluated by the use of the control module by subtracting a value of a second n-bit digital word from a value of a first n-bit digital word. A value one is assigned to bits of the first digital word if capacitors in the set of capacitors corresponding to these bits have been charged by the reference current source. A value zero is assigned to other bits of the first digital word. The inverted values of the first digital word are assigned to corresponding bits of the second digital word by the use of the control module. The value of n-bit output digital word is decreased by one if a voltage on the last capacitor charged by the reference current source has not reached the threshold voltage.

[0014] It is advantageous if a value representing n-bit output digital word being a conversion result is evaluated by the use of the control module in the following way. The control module assigns a value one to a bit in this digital word if a next capacitor is not started to be charged by the use of the signal current source during a time when a capacitor corresponding to the particular bit in the set of capacitors is charged by the use of the reference current source. The control module assigns also a value one to a bit in this digital word if, a next capacitor is started to be charged by the use of the reference current source during a time when a capacitor corresponding to the particular bit in the set of capacitors is charged by the use of the signal current source. The control module assigns a value zero to the bit otherwise.

[0015] An apparatus for conversion of a time interval to a digital word, according to the invention, comprising a control module having a time input, a digital output, a complete conversion output, a reference input connected to a reference comparator output, a signal input connected to a signal comparator output, a reference output connected to a control input of a reference current source, a signal output connected to a control input of a signal current source, and control outputs of change-over switches of a set of capacitors. A capacitance value of a capacitor of a given index is twice as high as a capacitance value of the capacitor of the previous index. A non-inverting input of the reference comparator is connected to a reference rail and to an output of the reference current source, whose input is connected to a source of a voltage supply. An inverting input of the reference comparator is connected to a source of a threshold voltage.

[0016] The essence of the apparatus, according to the invention, consists in that a non-inverting input of the signal comparator is connected to the signal rail and to the output of the signal current source whose input is connected to the source of the voltage supply. The inverting input of the signal comparator is connected to the source of the threshold voltage and to the inverting input of the reference comparator. Bottom plates of capacitors of the set of capacitors are connected to a ground of the circuit, and top plates of capacitors are connected respectively to moving contacts of change-over switches. First stationary contacts of the change-over switches are connected to the signal rail, second stationary contacts are connected to the ground of the circuit, and third stationary contacts are connected to the reference rail.

[0017] It is advantageous if the signal current source and the reference current source have the same intensity.

[0018] It is advantageous if intensity of the reference current source is controllable.

[0019] The advantage of the solution consists in that the operation of the apparatus is timed by two comparators which detect instants when particular conversion stages are completed. In this way a need of using an external source of timing signal that consumes considerable amount of energy is eliminated. Thereby, energy efficiency of conversion is improved.

[0020] High energy efficiency of method and apparatus, according to the invention, results also from the idle operation between conversion cycles because the solution consumes then less power if it is implemented in CMOS technology.

[0021] The permanent connection of bottom plates of all capacitors in a set of capacitors limits influence of parasitic capacitances on conversion accuracy, reduces a number of switches, and simplifies control of its operation.

[0022] The use of the reference current source with controlled intensity enables independent tuning of converter input range and the maximum length of the signal time. In this way, the conversion time of the converter can be reduced compared to the situation when the reference current source of fixed intensity equal to the signal current source is used.

[0023] The solution, according to the invention, is presented in the following figures:

Fig. 1 illustrates a schematic diagram of the apparatus in idle state before beginning of input time interval.
Fig. 2 illustrates a temporal relationship between an input time interval T, a reference time RT and a signal time ST.

[0024] The method for conversion of a time interval to a digital word using a successive approximation scheme, according to the invention, consists in determining a difference between a length of a reference time RT and a length of a signal time ST (Fig. 2). The reference time RT is generated from an instant t_1 when the beginning of the time interval T is detected by the use the control module CM. The signal time ST is generated from an instant t_2 when the end of the time interval T is detected by the use the control module CM.

[0025] The generation of the reference time RT and the signal time ST is terminated at the same instant t_3 when each capacitor in the set of capacitors was charged. A binary representation of the difference between the length of the reference time RT and the length of the signal time ST is assigned by the control module to the n-bit output digital word B.

[0026] The generation of the reference time RT is realized by charging a capacitor using a reference current source I_R. This capacitor is selected by the use of the control module CM from a set of capacitors CS comprising capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0. The capacitor C_{n-1} of the highest capacitance in the set of capacitors CS is selected first. A selected capacitor is charged as long as the reference voltage U_R increasing on the selected capacitor and compared to the threshold voltage U_{TH} by the use of the reference comparator K_R reaches the threshold voltage U_{TH}. Then, a next capacitor in the set of capacitors CS is started to be charged while this capacitor has the highest capacitance among the capacitors that have not been charged yet, and the reference voltage U_R increasing on this capacitor being charged is compared to the threshold voltage U_{TH} by the use of the reference comparator K_R. The cycle is repeated until all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 are charged. Intensity of the reference current source I_R and the signal current source I_S are fixed and the same. The generation of the signal time ST is realized by charging a capacitor by the use of the signal current source I_S. This capacitor selected by the use of the control module CM from a set of capacitors CS has the highest capacitance among the capacitors that have not been charged yet. The selected capacitor is charged as long as the signal voltage U_S increasing on this capacitor and compared to the threshold voltage U_{TH} by the use of the signal comparator K_S equals the threshold voltage U_{TH}. Then, a next capacitor in the set of capacitors CS is started to be charged by the use of the signal current source I_S, while this capacitor is selected in the same way. The cycle is repeated until all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 are charged.

[0027] The generation of the reference time RT and the generation of the signal time ST are terminated during the time when the capacitor C_0 of the lowest capacitance in the set of capacitors CS is charged, and when the reference voltage U_R increasing on a capacitor charged by the use of the reference current source I_R, or when the signal voltage U_R increasing on a capacitor charged by the use of the signal current source Is reaches the threshold voltage U_{TH}.

[0028] Another version of the method for conversion of a time interval to a digital word using a successive approximation scheme differs from the aforementioned version in that intensity of the reference current source I_R is twice lower than intensity of the signal current source Is during the time interval T. Intensity of the reference current source I_R is increased by the use of the control module CM to intensity of the signal current source Is at the instant t_2 when the generation of the time interval T is terminated by the use of the control module CM.

[0029] In both version of the method, a binary value represented by the n-bit output digital word B, being a conversion result, is evaluated by the use of the control module CM by subtracting a value of a second n-bit digital word from a value of a first n-bit digital word. A value one is assigned to bits of the first digital word if capacitors in the set of capacitors CS corresponding to these bits have been charged by the reference current source I_R, and a value zero is assigned to other bits of the first digital word. Inverted values of the first digital word are assigned to corresponding bits of the second digital word by the use of the control module CM. Finally, the binary value of n-bit output digital word B is decreased by one if a voltage on the last capacitor charged by the reference current source I_R has not reached the threshold voltage U_{TH}.

[0030] According to another version of the method, a binary value represented by the n-bit output digital word B, being a conversion result, is evaluated by the use of the control module CM such that the control module CM assigns a value one to a bit b_j in this digital word if a next capacitor C_{j-1} is not started to be charged by the use of the signal current source I_S during a time when a capacitor C_j corresponding to the bit b_j in the set of capacitors CS is charged by the use of the reference current source I_R, or a next capacitor C_{j-1} is started to be charged by the use of the reference current source I_R during a time when a capacitor C_j is charged by the use of the signal current source I_S. On the other hand, the control module CM assigns a value zero to the bit b_j otherwise.

[0031] In the first embodiment, an apparatus for conversion of a time interval to a digital word using a successive approximation scheme, according to the invention, comprises a control module CM having a time input In, a digital output B, a complete conversion output RDY. A reference input In_R of the control module CM is connected to an output of a reference comparator K_R, and a signal input In_S of the control module CM is connected to an output of a signal comparator K_S (Fig. 1). A reference output P_R of the control module CM is connected to a control input of a reference current source I_R, and a signal output Ps of the control module CM is connected to a control input of a signal current source I_S. Control

outputs P_{n-1}, P_{n-2}, ..., P_1, P_0 of the control module CM are connected respectively to control inputs of change-over switches S_{n-1}, S_{n-2}, ..., S_1, S_0 of a set of capacitors CS.

[0032] A capacitance value of each capacitor C_{n-1}, C_{n-2}, ..., C_1, C_0 of a given index in the set of capacitors CS is twice as high as a capacitance value of the capacitor of the previous index. A non-inverting input of the reference comparator K_R is connected to a reference rail R and to an output of the reference current source I_R, whose input is connected to a source of a voltage supply U_{DD}. An inverting input of the reference comparator K_R is connected to a source of a threshold voltage U_{TH}. A non-inverting input of the signal comparator K_S is connected to the signal rail S and to the output of the signal current source I_S whose input is connected to the source of the voltage supply U_{DD}. The inverting input of the signal comparator K_S is connected to the source of the threshold voltage U_{TH} and to the inverting input of the reference comparator K_R. Bottom plates of capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 of the set of capacitors CS are connected to a ground of a circuit, and top plates of the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 are connected respectively to moving contacts of change-over switches S_{n-1}, S_{n-2}, ..., S_1, S_0. First stationary contacts of the change-over switches S_{n-1}, S_{n-2}, ..., S_1, S_0 are connected to the signal rail S, second stationary contacts are connected to the ground of the circuit, and third stationary contacts are connected to the reference rail R. The signal current source Is and the reference current source I_R have the same intensity in the first embodiment.

[0033] In the second embodiment, the apparatus differs from the version presented in the first embodiment in that intensity of the reference current source I_R is controllable, and is changed by the reference output P_R of the control module CM.

[0034] The description below includes the following symbols:

x is an index of a capacitor actually charged by the use of the reference current source I_R,
y is an index of a capacitor actually charged by the use of the signal current source I_S,
z is an index of a capacitor having the highest capacitance among the capacitors in the set of capacitors that have not been charged yet.

[0035] The conversion of a time interval to a digital word using a successive approximation scheme according to invention in the first embodiment is realized as follows.

[0036] Before the start of the process of conversion, the control module CM causes the switching off the reference current source I_R by the use of the signal from the reference output P_R, and also the switching off the signal current source Is by the use of the signal from the signal output Ps. Additionally, by the use of signals from the control outputs P_{n-1}, P_{n-2}, ..., P_1, P_0, the control module CM causes the switching of change-over switches S_{n-1}, S_{n-2}, ..., S_1, S_0 and the connection of the top plates of the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the set of capacitors CS to the ground of the circuit enforcing a complete discharge of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the set of capacitors CS. At the instant t_1, when the control module CM detects the beginning of the time interval T on the input time interval In, the control module CM introduces the complete conversion output RDY to an inactive state. Next, the control module CM starts generation of the reference time RT (Fig. 2). Then, by the use of the signal from the control output P_{n-1}, the control module CM causes the switching of the change-over switch S_{n-1} and the connection of an output of the reference current source I_R to the top plate of the capacitor C_{n-1} having the highest capacitance in the set of capacitors CS. At the same time, by the use of the signal from the reference output P_R, the control module CM causes the switching on the reference current source I_R. Next, the control module assigns a value one to a bit b_{n-1} of the first n-bit digital word, and a value zero to a bit b_{n-1} of the second n-bit digital word. The reference voltage U_R increasing on a capacitor C_x charged by the use of the reference current source I_R is compared to the threshold voltage U_{TH} by the use of the reference comparator K_R. When the reference voltage U_R on the capacitor C_x reaches the threshold voltage U_{TH}, then, on the basis of the output signal of the reference comparator K_R, the control module CM by the use of the signal from the control output P_x causes the switching of the change-over switch S_x and the connection of the top plate of the capacitor C_x to the ground of the circuit enforcing a complete discharge of this capacitor. At the same time, the control module CM by the use of the signal from the control output P_z causes the switching of the change-over switch S_z and the connection of the output of the reference current source I_R to the top plate of the capacitor C_z such that it has the highest capacitance among the capacitors CS in the set of capacitors that have not been charged yet.

[0037] Next, the control module assigns a value one to a bit b_z of the first n-bit digital word, and a value zero to a bit b_z of the second n-bit digital word. The reference voltage U_R increasing on a capacitor C_x charged by the use of the reference current source I_R is compared to the threshold voltage U_{TH} by the use of the reference comparator K_R. The cycle is repeated until the generation of the reference time RT is terminated at the same instant t_3. At the instant t_2, when the control module CM detects the end of the time interval T on the input time interval In, the control module CM starts to generate the signal time ST (Fig. 2). Then, by the use of the signal from the control output P_z, the control module CM causes the switching of the change-over switch S_z and the connection of an output of the signal current source I_S to the top plate of the capacitor C_z such that it has the highest capacitance among the capacitors CS in the set of capacitors that have not been charged yet. At the same time, by the use of the signal from the signal output P_S, the

control module CM causes the switching on the signal current source I_S. Next, the control module assigns a value zero to a bit b_{n-1} of the first n-bit digital word, and a value one to a bit b_{n-1} of the second n-bit digital word. The signal voltage U_S increasing on a capacitor C_y charged by the use of the signal current source I_S is compared to the threshold voltage U_{TH} by the use of the signal comparator K_S. When the signal voltage U_S equals the threshold voltage U_{TH}, then, on the basis of the output signal of the reference signal K_S, the control module CM by the use of the signal from the control output P_y causes the switching of the change-over switch S_y and the connection of the top plate of the capacitor C_y to the ground of the circuit enforcing a complete discharge of this capacitor. At the same time, the control module CM by the use of the signal from the control output P_z causes the switching of the change-over switch S_z and the connection of the output of the signal current source I_S to the top plate of the capacitor C_z such that it has the highest capacitance among the capacitors CS in the set of capacitors that have not been charged yet. The cycle is repeated until generation of the signal time ST is terminated at the same instant t_3.

[0038] The generation of the reference time RT and the generation of the signal time ST are terminated by the control module CM at the instant t_3 (Fig. 2) when the capacitor C_0 of the lowest capacitance in the set of capacitors CS is charged, and when the control module CM on the basis of the output signal of the reference comparator K_R detects that the reference voltage U_R increasing on a capacitor C_x charged by the use of the reference current source I_R equals the threshold voltage U_{TH}, or when the control module CM on the basis of the output signal of the source comparator K_S detects that the signal voltage Us increasing on a capacitor C_y charged by the use of the signal current source I_S equals the threshold voltage U_{TH}. In the latter case, the value of the first n-bit digital word is decreases by one by use of the control module CM.

[0039] Next, in both cases, the control module CM by the use of the signal from the reference output Ps causes the switching off the reference current source I_R and by the use of the signal from the signal output P_S causes the switching off the signal current source I_S. Additionally, by the use of the signal from the control outputs P_{n-1}, P_{n-2}, ..., P_1, P_0, the control module CM causes the switching of the change-over switches S_{n-1}, S_{n-2}, ..., S_1, S_0 and the connection of the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 to the ground of the circuit enforcing a complete discharge of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the set of capacitors CS. The control module CM evaluates values of bits b_{n-1}, b_{n-2}, ..., b_1, b_0 in the n-bit output digital word B subtracting a value of the second n-bit digital word from a value of the first n-bit digital word. Next, the control module CM introduces the complete conversion output RDY to an active state.

[0040] In the second embodiment, the apparatus for conversion of a time interval to a digital word using a successive approximation scheme differs from the version presented in aforementioned example in that the control module CM by the use of the control signal from the reference output P_R causes a decrease of intensity of the reference current source I_R below intensity of the signal current source I_S at the instant t_1, when the control module CM detects the beginning of the time interval T on the input time interval In. At the instant t_2, when the control module CM detects the end of the time interval T on the input time interval In, the control module CM by the use of the control signal from the reference output P_R causes an increase of intensity of the reference current source I_R to intensity of the signal current source Is.

[0041] In another embodiment, the control module CM evaluates values of bits b_{n-1}, b_{n-2}, ..., b_1, b_0 in the n-bit output digital word B as a conversion result by assigning a value one to a bit b_x in this digital word B if, a next capacitor C_{x-1} is not started to be charged by the use of the signal current source I_S during a time when a capacitor C_x corresponding to the bit b_x in the set of capacitors CS is charged by the use of the reference current source I_R, or, a next capacitor C_{y-1} is started to be charged by the use of the reference current source I_R during a time when a capacitor C_y corresponding to the bit b_y in the set of capacitors CS is charged by the use of the signal current source I_S. Otherwise, the control module CM assigns a value zero to the bits in this digital word B.

Acronims

[0042]

In	time input
In_S	signal input
In_R	reference input
P_S	signal output
P_R	reference output
B	digital output
b_{n-1}, b_{n-2}, ..., b_1, b_0	bits of digital output
RDY	complete conversion output
Is	signal current source
I_R	reference current source
S	signal rail
R	reference rail

Ks	signal comparator
K_R	reference comparator
CS	set of capacitors
C_{n-1}, C_{n-2}, ..., C_1, C_0	capacitors
C_{n-1}	capacitor having the highest capacitance in the set of capacitors
C_0	capacitor having the lowest capacitance in the set of capacitors
S_{n-1}, S_{n-2}, ..., S_1, S_0	change-over switches
P_{n-1}, P_{n-2}, ..., P_1, P_0	control outputs
CM	control module
U_S	signal voltage
U_R	reference voltage
U_{TH}	threshold voltage
U_{DD}	supply voltage
T	time interval
t_1	instant when the beginning of the time interval T is detected
t_2	instant when the end of the time interval T is detected
t_3	instant when generation of the reference time RT and the signal time ST is terminated
ST	signal time
RT	reference time

Claims

1. A method for conversion of a time interval to a digital word using a successive approximation scheme consisting in a detection of a beginning and of an end of the time interval (T) by the use of a control module (CM), and in assignment of a corresponding binary value represented by n-bit output digital word (B) to the time interval by the use of the control module (CM), **characterized in that** the time interval (T) is mapped to a difference of a length of a reference time (RT) and a length of a signal time (ST), while the reference time (RT) is generated from an instant (t_1) when the beginning of the time interval (T) is detected by the use of the control module (CM), and the signal time (ST) is generated from an instant (t_2) when the end of the time interval (T) is detected by the use the control module (CM), whereas generation of the reference time (RT) and the signal time (ST) is terminated at the same instant (t_3) and a generation of the reference time (RT) is realized by charging a capacitor using a reference current source (I_R), while this capacitor is selected by the use of the control module (CM) from a set of capacitors (CS) comprising capacitors (C_{n-1}, C_{n-2}, ..., C_1, C_0), such that a capacitance of a capacitor of a given index is twice as high as a capacitance of a capacitor of the previous index, and a capacitor (C_{n-1}) of the highest capacitance in the set of capacitors (CS) is selected first, while the selected capacitor is charged as long as a reference voltage (U_R) increasing on the selected capacitor and compared to a threshold voltage (U_{TH}) by the use of a reference comparator (K_R) reaches the threshold voltage (U_{TH}), and then, a next capacitor in the set of capacitors (CS) is started to be charged while this capacitor has the highest capacitance among the capacitors that have not been charged yet, and the reference voltage (U_R) increasing on this capacitor being charged is compared to the threshold voltage (U_{TH}) by the use of the reference comparator (K_R), and the cycle is repeated to the end of generation of both time intervals, while generation of the signal time (ST) is realized by charging a capacitor by the use of a signal current source (I_S), while this capacitor is selected by the use of the control module (CM) from the set of capacitors (CS) having the highest capacitance among the capacitors that have not been charged yet, and the selected capacitor is charged as long as a signal voltage (U_S) increasing on this capacitor and compared to the threshold voltage (U_{TH}) by the use of a signal comparator (K_S) reaches the threshold voltage (U_{TH}), and then, a next capacitor in the set of capacitors (CS) is started to be charged by the use of a signal current source (I_S) while this capacitor is selected in a similar way as for the selection of a next capacitor for the above-mentioned generation of the reference time (RT) and the cycle is repeated, and the generation of the reference time (RT) and the generation of the signal time (ST) are terminated during the time when the capacitor (C_0) of the lowest capacitance in the set of capacitors (CS) is charged, and when the reference voltage (U_R) increasing on a capacitor charged by the use of the reference current source (I_R), or when the signal voltage (U_S) increasing on a capacitor charged by the use of the signal current source (I_S) reaches the threshold voltage (U_{TH}).

2. Method as claimed in claim 1, **characterized in that** an intensity of the reference current source (I_R) is lower than an intensity of the signal current source (I_S) during the time interval (T), and the intensity of the reference current source (I_R) is increased by the use of the control module (CM) to intensity the signal current source (I_S) at the instant (t_2) when generation of the time interval (T) is terminated by the use of the control module (CM).

3. Method as claimed in claim **1** and claim 2, **characterized in that** the binary value represented by an n-bit output digital word (B) is evaluated by the use of the control module (CM) by subtracting a value of a second n-bit digital word from a value of a first n-bit digital word, while a value one is assigned to bits of the first digital word if capacitors in the set of capacitors (CS) corresponding to these bits have been charged by the reference current source (I_R), and a value zero is assigned to other bits of the first digital word, whereas the inverted values of the first digital word are assigned to corresponding bits of the second digital word by the use of the control module (CM), and finally the value of n-bit output digital word (B) is decreased by one if a voltage on the last capacitor charged by the reference current source (I_R) has not reached the threshold voltage (U_{TH}).

4. Method as claimed in claim **1** and claim 2, **characterized in that** a binary value of an n-bit output digital word (B) is evaluated by the use of the control module (CM) such that the control module (CM) assigns a value one to a bit (b_j) in this digital word if, a next capacitor (C_{j-1}) is not started to be charged by the use of the signal current source (I_S) during a time when a capacitor (C_j) corresponding to the bit (b_j) in the set of capacitors (CS) is charged by the use of the reference current source (I_R), or, a next capacitor (C_{j-1}) is started to be charged by the use of the reference current source (I_R) during a time when a capacitor (C_j) corresponding to the bit (b_j) in the set of capacitors (CS) is charged by the use of the signal current source (I_S), while the control module (CM) assigns a value zero to the bit (b_j) otherwise.

5. An apparatus for conversion of a time interval to a digital word using a successive approximation scheme comprising a control module (CM) having a time input (In), a digital output (B), a complete conversion output (RDY), a reference input (Inr) connected to a reference comparator output, a signal input (Ins) connected to a signal comparator output, a reference output (P_R) connected to a control input of a reference current source (I_R), a signal output (P_S) connected to a control input of a signal current source (I_S), and outputs (P_{n-1}, P_{n-2}, ..., P_1, P_0) that control change-over switches (S_{n-1}, S_{n-2}, ..., S_1, S_0) of a set of capacitors (C_{N-1}, C_{N-2}, ..., C_1, C_0), while a capacitance value of a capacitor of a given index is twice as high as a capacitance value of the capacitor of the previous index, and a non-inverting input of the reference comparator (K_R) is connected to a reference rail (R) and to an output of the reference current source (I_R), whose input is connected to a source of a voltage supply (U_{DD}), and an inverting input of the reference comparator (K_R) is connected to a source of a threshold voltage (U_{TH}), **characterized in that** a non-inverting input of the signal comparator (K_S) is connected to a signal rail (S) and to the output of the signal current source (I_S) whose input is connected to the source of the voltage supply (U_{DD}), and the inverting input of the signal comparator (K_S) is connected to the source of the threshold voltage (U_{TH}) and to the inverting input of the reference comparator (K_R), while bottom plates of capacitors (C_{n-1}, C_{n-2}, ..., C_1, C_0) of the set of capacitors (CS) are connected to a ground of the apparatus, and top plates of capacitors (C_{n-1}, C_{n-2}, ..., C_1, C_0) are connected respectively to moving contacts of change-over switches (S_{n-1}, S_{n-2}, ..., S_1, S_0) whose first stationary contacts are connected to the signal rail (S), second stationary contacts are connected to the ground of the apparatus, and third stationary contacts are connected to the reference rail (R).

6. Apparatus as claimed in claim 5, **characterized in that** the signal current source (I_S) and the reference current source (I_R) have the same intensity.

7. Apparatus as claimed in claim 5, **characterized in that** intensity of the reference current source (I_R) is controllable.

Patentansprüche

1. Verfahren zur Umwandlung eines Zeitintervalls in digitales Wort durch Schema der schrittweisen Annäherung, die in der Entdeckung mittels des Steuerungsmoduls (CM) des Anfangs und des Endes des Zeitintervalls (T) sowie der Zuschreibung dem Zeitintervall mittels des Steuerungsmoduls (CM) des entsprechenden binaren Wertes des digitalen n-Bit Ausgangswort (B) besteht, **dadurch gekennzeichnet, dass** sich das Zeitintervall (T) mithilfe des Steuerungsmoduls (CM) in der Form der Längendifferenz des Abschnittes der Referenzzeit (RT) und des Abschnittes der Signalzeit (ST) abbildet, wobei der Abschnitt der Referenzzeit (RT) wird ab dem Zeitpunkt (t_1) der Entdeckung mittels des Steuerungsmoduls (CM) des Anfangs des Zeitintervalls (T) und der Abschnitt der Signalzeit (ST) ab dem Zeitpunkt (t_2) der Entdeckung mittels des Steuerungsmoduls (CM) des Endes des Zeitintervalls (T) gemessen, die Messung des Abschnitts der Referenzzeit (RT) und des Abschnittes der Signalzeit (ST) endet zu demselben Zeitpunkt (t_3), die Messung des Abschnitts der Referenzzeit (RT) wird durch das Laden realisiert, mithilfe der Referenzstromquelle (I_R), des Kondensators, der mithilfe des Steuerungsmoduls (CM) unter dem Satz an Kondensatoren (CS) gewählt wird, welcher solche Kondensatoren (C_{n-1}, C_{n-2}, ..., C_1, C_0) enthält, dass das Volumen von jedem Kondensator mit nächstem Index doppelt so groß ist wie das Volumen des unmittelbar früheren Kondensators und

als erstes wird der Kondensator (C_{n-1}) mit dem höchsten Volumen in dem Satz an Kondensatoren (CS) ausgewählt, wobei der ausgewählte Kondensator bis zu dem Zeitpunkt geladen wird, wenn die in ihm steigende Referenzspannung (U_R), die mithilfe des Referenzkomparators (K_R) mit der Schwellenspannung (U_{TH}) verglichen wird, gleich der Schwellenspannung (U_{TH}) ist und dann beginnt das Laden des nächsten, aus dem Satz der Kondensatoren (CS) gewählten Kondensators so, dass das Volumen dieses Kondensators das größte unter den noch nicht geladenen Kondensatoren ist, und die darin steigende Referenzspannung (U_R) mithilfe des Referenzkomparators (K_R) mit der Schwellenspannung (U_{TH}) verglichen wird und man diese Handlungen bis zur Beendigung beider Zeitintervalle wiederholt, die Messung des Abschnittes der Signalzeit (ST) wird durch das Laden mithilfe der Signalstromquelle (Is) des mittels des Steuerungsmoduls (CM) unter dem Satz der Kondensatoren (CS) solchen ausgewählten Kondensators realisiert, dass das Volumen dieses Kondensators das größte unter den noch nicht geladenen Kondensatoren ist, wobei der ausgewählte Kondensator bis zu dem Zeitpunkt geladen wird, wenn die darin steigende Signalspannung (Us), die mittels des Signalkomparatoren (K_s) mit der Schwellenspannung (U_{TH}) verglichen wird, mit der Schwellenspannung (U_{TH}) gleich ist, daraufhin beginnt das Laden mittels der Signalstromquelle (Is) des nächsten Kondensators, der auf dieselbe Art und Weise gewählt wird, wie die Wahl des Kondensators, der für die oben genannte Messung der Referenzzeit (RT) bestimmt ist und diese Handlungen wiederholt man, bis die Messung des Abschnittes der Referenzzeit (RT) und des Abschnittes der Signalzeit (ST) endet, wenn während des Ladens des Kondensators (C_0) mit dem geringsten Volumen im Satz (CS) entdeckt wird, dass die Referenzspannung (U_R), die auf dem mithilfe der Referenzstromquelle (I_R) geladenen Kondensator steigt oder die Signalspannung (U_S), die auf dem mithilfe der Signalstromquelle (I_S) geladenen Kondensator steigt, der Schwellenspannung (U_{TH}) gleich ist.

2. Verfahren nach dem Anspruch 1, **dadurch gekennzeichnet, dass** die Leistungen der Referenzstromquelle (I_R) während der Dauer des Zeitintervalls (T) kleiner als die Leistung der Signalstromquelle (I_s) ist, und zum Zeitpunkt (t_2) der Entdeckung mittels des Steuerungsmoduls (CM), bis zum Ende des Zeitintervalls (T) sich diese Leistung mittels des Steuerungsmoduls (CM), bis zu der Leistung der Signalstromquelle (I_s) erhöht.

3. Verfahren nach dem Anspruch 1, **dadurch gekennzeichnet, dass** der binare Wert des digitalen n-Bit Ausgangswortes, der das Ergebnis der Umwandlung ist, mithilfe des Steuerungsmoduls (CM) durch das Subtrahieren von dem Wert des ersten digitalen n-Bit Wortes des Wertes des zweiten digitalen n-Bit Wortes bestimmt wird, wobei den Bits des ersten digitalen Wortes der Wert eins (1) zugeschrieben wird, wenn die ihnen zugeschriebene Kondensatoren des Satzes an den Kondensatoren (CS) mithilfe der Referenzstromquelle (I_R) geladen wurden, und den übrigen Bits dieses Wortes der Wert Null (0) zugeschrieben wird, den Bits des zweiten digitalen Wortes werden mithilfe des Steuerungsmoduls (CM) negierte Werte der Bits des ersten digitalen Wortes zugeschrieben, auf diese Art und Weise bestimmte Wert des digitalen n-Bit Ausgangswortes (B) vermindert man um eins (1), wenn der letzte von den Kondensatoren, der mithilfe der Referenzstromquelle (I_R) geladen wurde, nicht bis auf die Spannung geladen wurde, die der Schwellenspannung (U_{TH}) gleich ist.

4. Verfahren nach dem Anspruch 1 und 2, **dadurch gekennzeichnet, dass** der binare Wert des digitalen Ausgangswortes (B) mithilfe des Steuerungsmoduls (CM) bestimmt wird, indem man dem Bit (b_j) dieses digitalen Wortes der Wert eins (1) zugeschrieben wird, wenn man das Laden des nächsten Kondensators (C_{j-1}) mithilfe der Signalstromquelle (I_S) während des Ladens des Kondensators (C_j), der diesem Bit zugeordnet ist, in dem Satz der Kondensatoren (CS) mithilfe der Referenzstromquelle (I_R) nicht angefangen hat oder man mit dem Laden des nächsten Kondensators (C_{j-1}) mithilfe der Referenzstromquelle (I_R) während des Ladens des Kondensators (C_j), der diesem Bit zugeordnet ist, in dem Satz der Kondensatoren mithilfe der Signalstromquelle (I_S) angefangen hat, dagegen in den übrigen Fällen schreibt das Steuerungsmodul (CM) diesem Bit (b_j) den Wert Null (0) zu.

5. Vorrichtung zur Umwandlung eines Zeitintervalls in digitales Wort durch Schema der schrittweisen Annäherung, die das Steuerungsmodul (CM) enthält, das mit folgenden Elementen ausgestattet ist: der Eingang des Zeitintervalls (In), Ausgang des digitalen Wortes (B), Ausgang des Abschlusses der Umwandlung (RDY), Referenzeingang (Inr), der mit dem Ausgang des Referenzkomparators verbunden ist und Signaleingang (Ins), der mit dem Ausgang des Signalkomparators verbunden ist, Referenzausgang (PR), der mit dem Steuerungseingang der Referenzstromquelle (IR) verbunden ist, Signalausgang (PS), verbunden mit dem Steuerungsausgang der Signalstromquelle (IS) verbunden ist, wie auch die Ausgänge (P_{n-1}, P_{n-2},...P_1, P_0), die die Umschalter ($S_{n-}1$, $S_{n-}2$,...S_1, S_0) des Satzes an Kondensatoren (C_{n-1}, C_{n-2},...C_1, C_0) steuern, wobei das Volumen von jedem Kondensator mit nächstem Index doppelt so groß ist wie das Volumen des unmittelbar früheren Kondensators, und darüber hinaus nichtumleitender Eingang des Referenzkomparators (K_R) ist mit der Referenzschiene (R) sowie dem Ausgang der Referenzstromquelle (I_R) verbunden, deren Eingang ist mit der Spannungsversorgungsquelle (U_{DD}) verbunden, und der umleitende Eingang des Referenzkomparators (K_R) ist mit der Quelle der Schwellenspannung (U_{TH}) verbunden, **dadurch gekennzeichnet, dass** nichtumleitender Eingang des Signalkomparators (K_S) ist mit der Signalschiene (S) sowie

dem Ausgang der Signalstromquelle (I_S) verbunden, deren Eingang ist mit der Spannungsversorgungsquelle (U_{DD}) verbunden, und der umleitende Eingang des Signalkomparators (K_S) ist mit der Quelle der Schwellenspannung (U_{TH}), sowie mit dem umleitenden Eingang des Referenzkomparators (K_R) verbunden, und die unteren Platten der Kondensatoren ($C_{n-}1$, C_{n-2},...C_1, C_0) des Satzes an Kondensatoren (CS) mit der Masse der Schaltung verbunden sind, und die oberen Platten dieser Kondensatoren (C_{n-1}, $C_{n-}2$,...C_1, C_0) entsprechend mit den beweglichen Kontaktstücken der Umschalter (S_{n-1}, S_{n-2},...S_1, S_0) verbunden sind, derer erste unbeweglichen Kontaktstücke mit der Signalschiene (S), zweite unbeweglichen Kontaktstücke mit der Masse der Schaltung und dritte unbeweglichen Kontaktstücke mit der Referenzschiene (R) verbunden sind.

6. Vorrichtung nach dem Anspruch 5, **dadurch gekennzeichnet, dass** die Signalstromquelle (I_S) und die Referenzstromquelle (I_R) die gleiche Leistung haben.

7. Vorrichtung nach dem Anspruch 5, **dadurch gekennzeichnet, dass** die Referenzstromquelle (I_R) einstellbare Leistung hat.

Revendications

1. Procède de conversion d'intervalle de temps en mot numérique utilisant un schéma d'approximations successives, qui consiste à détecter le début et la fin de l'intervalle de temps (T) à l'aide du module de commande (CM) et à attribuer à l'intervalle de temps la valeur binaire n-bits appropriée du mot numérique de sortie (B), à l'aide du module de commande (CM), **caractérisé en ce que** l'intervalle de temps (T) est représenté à l'aide du module de commande (CM) sous la forme de la différence de longueur du segment de temps de référence (RT) et du segment de temps de signal (ST), où le segment de temps de référence (RT) se mesure à partir de l'instant (t_1) de détection par le module de commande (CM) du début de l'intervalle de temps (T), et un segment de temps de signal (ST) se mesure à partir de l'instant (t_2) de détection par le module de commande (CM) de la fin de l'intervalle de temps (T), tandis que la mesure du segment de temps de référence (RT) et du segment de temps de signal (ST) se termine au même instant (t_3), la mesure du segment de temps de référence (RT) est effectuée en chargeant avec la source référence de courant (I_R), du condensateur sélectionné à l'aide du module de commande (CM) de la batterie de condensateurs (CS) contenant des condensateurs (C_{n-1}, C_{n-2}, ..., C_1, C_0), tels que la capacité de chaque condensateur avec l'indice suivant est le double de la capacité du condensateur qui le précède immédiatement, et est choisi comme premier condensateur (C_{n-1})) celui avec la plus grande capacité de la batterie de condensateurs (CS), où le condensateur sélectionné est chargé jusqu'à ce que la tension de référence (U_R) qui s'accumule dessus, que l'on compare au moyen d'un comparateur de référence (K_R) à la tension de seuil (U_{TH}) soit égale à la tension de seuil (U_{TH}) alors la charge d'un autre condensateur sélectionné dans la batterie de condensateurs (CS) commence, de sorte que la capacité de ce condensateur est la plus grande parmi les condensateurs encore non chargés, et la tension de référence (U_R) qui s'accumule dessus est comparée à la tension de seuil (U_{TH}) à l'aide d'un comparateur de référence (K_R) et ces les étapes sont répétées jusqu'à ce que les deux intervalles de temps soient terminés, la mesure du segment de temps de signal (ST) est accomplie en chargeant, avec la source de courant de signal (I_S), un condensateur sélectionné à l'aide du module de commande (CM) à partir de la batterie de condensateurs (CS) de telle sorte que la capacité de ce condensateur soit la plus grande parmi les condensateurs non encore chargés, où le condensateur sélectionné est chargé jusqu'à ce que la tension de signal (U_S) qui s'y accumule, qui est comparée à la tension de seuil (U_{TH}) à l'aide du comparateur de signal (K_S), soit égale à la tension de seuil (U_{TH}), puis commence le chargement, à l'aide de la source de courant de signal (I_S), d'un autre condensateur, qui est sélectionné de la même manière que la sélection du condensateur destiné à la mesure du temps de référence (RT) susmentionnée et ces opérations se répètent, la mesure du segment de temps de référence (RT) et du segment de temps de signal (ST) se termine lorsqu'on détecte, pendant le chargement du condensateur (C_0) de la plus petite capacité dans la batterie (CS), que la tension de référence (U_R) augmentant aux bornes du condensateur chargé à l'aide de la source de courant de référence (I_R) ou la tension de signal (U_S) augmentant aux bornes du condensateur chargé à l'aide de la source de courant de signal (I_S) est égale à la tension de seuil (U_{TH}).

2. Procédé selon la revendication 1, **caractérisé en ce que** le rendement de la source de courant de référence (I_R) sur la durée de l'intervalle de temps (T) est inférieur au rendement de la source de courant de signal (I_S), et à l'instant (t_2) de détection, à l'aide du module de contrôle (CM), de la fin de l'intervalle de temps (T), cette capacité est augmentée par le module de contrôle (CM), à la capacité de la source de courant de signal (I_S).

3. Procédé selon la revendication 1, **caractérisé en ce que** la valeur binaire n-bits du mot numérique de sortie (B) résultant du traitement, est déterminée par le module de commande (CM) en soustrayant la valeur n-bits du deuxième

mot numérique à la valeur n-bits du premier mot numérique, où les bits du premier mot numérique reçoivent la valeur un (1) si les condensateurs de la batterie de condensateurs (CS) qui leur sont associés étaient chargés à l'aide de la source de courant de référence (I_R), et les bits restants de ce mot reçoivent la valeur zéro (0), tandis qu' on affecte aux bits du deuxième mot numérique, à l'aide du module de commande (CM), les valeurs de bits inversées du premier mot numérique, et la valeur de n-bit du premier mot numérique de sortie (B) ainsi déterminée est diminuée de un (1), si le dernier des condensateurs chargés à l'aide de la source de courant de référence (I_R) n'a pas été chargé à une tension égale à la tension de seuil (U_{TH}).

4. Procédé selon les revendications 1 et 2, **caractérisé en ce que** la valeur binaire n-bits du mot numérique de sortie (B) est déterminée à l'aide du module de commande (CM) affectant au bit (b_j) de ce mot numérique la valeur un (1) si aucun chargement du condensateur suivant (C_{j-1}) n'a commencé, à l'aide de la source de courant de signal (I_S) lorsque la charge du condensateur (C_j) associé à ce bit (b_j) dans la batterie de condensateurs (CS), à l'aide de la source de courant de référence (I_R), ou que la charge d'un autre condensateur (C_{j-1}) a débuté à l'aide de la source de courant de référence (I_R) lors de la charge du condensateur (Cj) associé à ce bit (b_j) dans la batterie de condensateurs (CS) à l'aide de la source de courant de signal (I_S), tandis que dans les autres cas, le module de commande (CM) attribue au bit (bj) une valeur de zéro (0).

5. Appareil de conversion d'un intervalle de temps en mot numérique par utilisant un schéma d'approximations successives, comprenant un module de commande (CM) équipé d'une entrée d'intervalle de temps (In), d'une sortie de mot numérique (B), d'une sortie de fin de traitement (RDY), d'une entrée de référence (Inr) connectée à la sortie du comparateur de référence et d'une entrée de signal (Ins) connectée à la sortie du comparateur de signal, d'une sortie de référence (P_R) connectée à l'entrée de commande de la source de courant de référence (I_R), d'une sortie de signal (Ps) connectée à l'entrée de commande de la source de courant de signal (Is) et des sorties (P_{n-1}, P_{n-2}, ..., P_1, P_0) commandant les interrupteurs (S_{n-1}, S_{n-2}, ..., S_1, S_0) de la batterie de condensateurs (C_{n-1}, C_{n-2}, ..., C_1, C_0) où dans un ensemble de condensateurs, la capacité de chaque condensateur avec l'indice suivant est le double de la capacité du condensateur qui le précède immédiatement ; de plus, l'entrée non-inverseuse du comparateur de référence (K_R) est reliée au rail de référence (R) et à la sortie de la source de courant de référence (I_R) dont l'entrée est connectée à la source d'alimentation (U_{DD}) et l'entrée inverseuse du comparateur de référence (K_R) est connectée à une source de tension de seuil (U_{TH}), **caractérisée en ce que** l'entrée non-inverseuse du comparateur de signal (K_S) est connectée au rail de signal (S) et à la sortie de la source de courant de signal (I_S), dont l'entrée est connectée à la source de tension d'alimentation (U_{DD}), et l'entrée inverseuse du comparateur de signal (K_S) est reliée à la source de la tension de seuil (U_{TH}) et à l'entrée inverseuse du comparateur de référence (K_R) tandis que les plaques inférieures des condensateurs (C_{n-1}, C_{n-2}, ..., C_1, C_0) de la batterie de condensateurs (CS) sont connectées à la masse du circuit, et les plaques supérieures de ces condensateurs (C_{n-1}, C_{n-2}, ..., C_1, C_0) sont connectées, respectivement, aux contacts mobiles des interrupteurs (S_{n-1}, S_{n-2}, ..., S_1, S_0), dont les premiers contacts fixes sont connectés au rail de signal (S), les seconds contacts fixes sont connectés à la masse du système et les troisièmes contacts fixes sont connectés au rail de référence (R).

6. Appareil selon la revendication 5, **caractérisé en ce que** la source de courant de signal (I_S) et la source de courant de référence (I_R) ont la même capacité.

7. Appareil selon la revendication 5, **caractérisé en ce que** la source de courant de référence (I_R) a une capacité régulée.

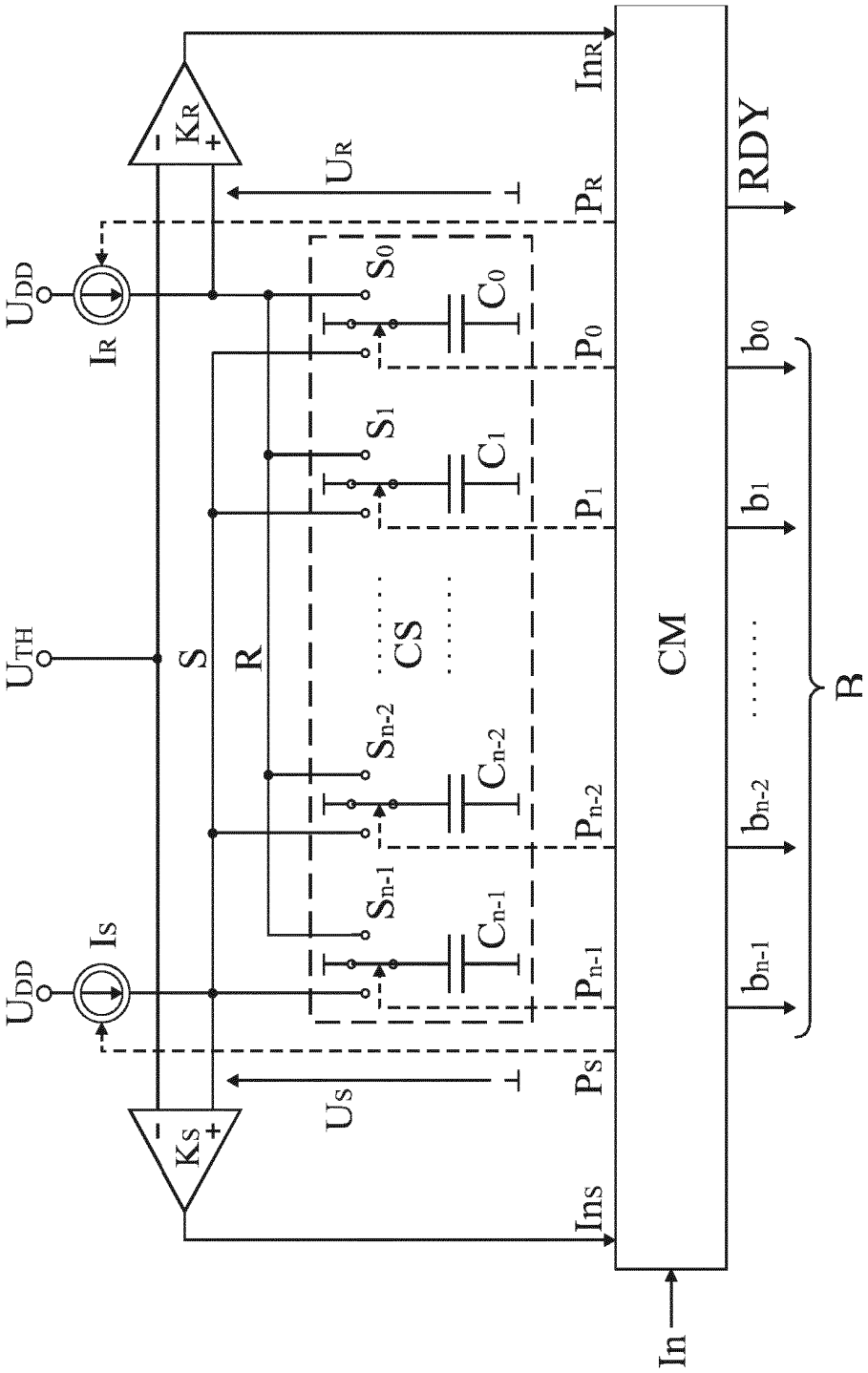
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Fig. 1

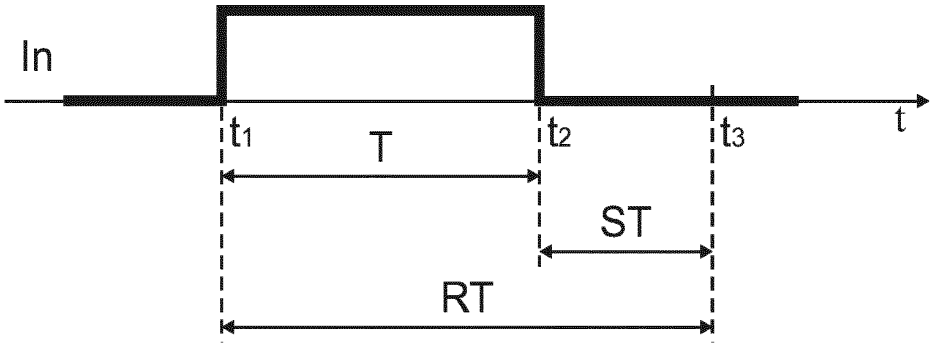

Fig. 2

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 9063518 B **[0002] [0005]**
- WO 2011152744 A **[0002] [0005]**