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Verfahren und Vorrichtung für taktgeberfreie Umwandlung eines Zeitintervalls in ein digitales Wort
Procédé et appareil de conversion sans horloge d'un intervalle de temps en mot numérique

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Description

[0001] The subject of this invention is a method and an apparatus for clockless conversion of a time interval to a digital word that can be applied in monitoring and control systems.

[0002] The method for the anachronous conversion of a voltage value to a digital word known from WO/2011/152744 consists in mapping a converted time interval to a portion of electric charge proportional to this time interval. A given portion of charge is delivered by the use of the current source during the converted time interval and is accumulated in the sampling capacitor. Accumulation of electric charge is realized until the end of the time interval is detected. Then, the accumulated electric charge is submitted to the process of redistribution by deploying the charge in the array of capacitors while a capacitance value of each capacitor of a given index is twice as high as a capacitance value of a capacitor of the previous index. During the process of redistribution, the accumulated electric charge is deployed in the capacitors in the array in a way that the obtained voltage equals zero, or equals the reference voltage on each capacitor or on each capacitor with the possible exception of one of capacitors. The course of the process of redistribution is controlled by means of the control module on the basis of output signals of the first and of the second comparator. Electric charge is delivered during the process of its accumulation by the use of the first current source and is transferred between capacitors during the process of its redistribution by the use of the second current source. By means of the control module, the value one is assigned to these bits in the digital word that correspond to capacitors on which voltage equal to the reference voltage value has been obtained and the value zero is assigned to the other bits in the digital word.

[0003] In one of variants of this solution, electric charge is accumulated simultaneously in the sampling capacitor and in the capacitor of the highest capacitance value in the array of capacitors which is connected to the sampling capacitor in parallel.

[0004] The apparatus for the asynchronous conversion of a time interval to a digital word is also known from WO/2011/152744. This apparatus comprises the array of capacitors whose control inputs are connected to the set of control outputs of the control module. The control module is equipped with the digital output, the complete conversion signal output, the time interval signal input and two control inputs. The first control input of the control module is connected to the output of the first comparator whose inputs are connected to one pair of outputs of the array of capacitors. The other control input of the control module is connected to the output of the second comparator whose inputs are connected to the other pair of outputs of the array. Furthermore, the voltage supply, the source of auxiliary voltage together with the source of the reference voltage, the sampling capacitor and two controlled current sources whose control inputs are con-

nected to the relevant control outputs of the control module. The array of capacitors comprises on-off switches, change-over switches and the array of capacitors whose number equals the number of bits in the digital word and a capacitance value of a capacitor of a given index is twice as high as a capacitance value of a capacitor of the previous index. The top plate of the sampling capacitor and the top plate of each capacitor in the array of capacitors are connected through the first on-off switch to the first rail and/or through the second on-off switch to the second rail and the bottom plate is connected through a change-over switch to ground of a circuit or to the source of auxiliary voltage. The first rail is connected to ground of the circuit through the first rail on-off switch and to the non-inverting input of the second comparator whose inverting input is connected to the source of the reference voltage. The second rail is connected to the inverting input of the first comparator whose non-inverting input is connected to the source of auxiliary voltage.

5 The control inputs of the first on-off switches and the control inputs of the change-over switches in the array of capacitors are coupled together and connected appropriately to the control outputs of the control module while the control inputs of the second on-off switches and the
10 control input of the first on-off switch are connected appropriately to the control outputs of the control module. The one end of the first current source is connected to the voltage supply and the one end of the second current source is connected to the second rail. The other end of
15 the first current source and the other end of the second current source are connected to the first rail.

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[0005] In one of variants of the abovementioned apparatus, the sampling capacitor whose capacitance value is not smaller than the capacitance value of the capacitor having the highest capacitance value in the array of capacitors is connected in parallel to the capacitor of the highest capacitance value in the array of capacitors. The conversion of a time interval to the digital word is realized by changing states of signals from the relevant control
25 outputs by means of the control module.

[0006] The invention relates to a method for clockless conversion of time interval to digital word according to claim 1 and to an apparatus for clockless conversion of time interval to digital word according to claim 5.

[0007] According to the invention, the method for clockless conversion of a time interval to a digital word consists in that the beginning and the end of a time interval are detected by the use of the control module and this time interval is mapped by a portion of electric charge which is proportional to this time interval. Electric charge is delivered during the converted time interval by the use of the current source and accumulated in the sampling capacitor, or in the sampling capacitor and in the capacitor of the highest capacitance value in the array of redistribution. Then, the process of redistribution of the accumulated electric charge is realized in the array of redistribution in a known way by changing states of signals from the relevant control outputs by the use of the control
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module and the relevant values are assigned to bits in the digital word by means of the control module. The array of redistribution comprises the set of on-off switches, the set of change-over switches and the set of capacitors while a capacitance value of each capacitor of a given index is twice as high as a capacitance value of a capacitor of the previous index.

[0008] The essence of the method, according to the invention, consists in that as soon as accumulation of electric charge is terminated in the sampling capacitor, or in the sampling capacitor and in the capacitor of the highest capacitance value in the array of redistribution, which is connected to the sampling capacitor in parallel, and as soon as the beginning of next time interval is detected by means of the control module, electric charge is delivered by the use of the current source and accumulated in an additional sampling capacitor. Next the process of redistribution of electric charge accumulated in the additional sampling capacitor is realized and the relevant values are assigned to bits in the digital word by means of the control module. The accumulation of electric charge in the additional sampling capacitor, the process of redistribution of electric charge accumulated in the additional sampling capacitor and assignment of the relevant values to bits in the digital word by means of the control module are realized as for the sampling capacitor.

[0009] In this method, it is possible that as soon as the accumulation of electric charge is terminated in the additional sampling capacitor and as soon as the beginning of the time interval is detected by means of the control module, the next cycle begins and electric charge is delivered by the use of the current source and accumulated again in the additional sampling capacitor, or in the sampling capacitor and in the capacitor of the highest capacitance value in the array of redistribution, which is connected to the sampling capacitor in parallel.

[0010] In this method, it is possible that in a period of time when electric charge is delivered by the use of the current source and accumulated in the additional sampling capacitor, a part of delivered electric charge is accumulated simultaneously in the additional capacitor having the highest capacitance value in the array of redistribution which is connected to the additional sampling capacitor in parallel. A capacitance value of the additional capacitor having the highest capacitance value in the array of redistribution equals the capacitance value of the capacitor having the highest capacitance value in the array of redistribution.

[0011] In this method, it is also possible that as soon as the process of redistribution is terminated, the portion of electric charge, accumulated in the last of capacitors on which reference voltage had not been reached when the process of redistribution was realized, is conserved. This portion of electric charge is taken into account when the next process of redistribution is realized.

[0012] The apparatus, according to the invention, comprises the array of redistribution whose control inputs are connected to control outputs of the control module. The

control module is equipped with the digital output, the complete conversion signal output, the trigger input, the first control input which is connected to the output of the first comparator and the other control input which is connected to the output of the second comparator. The source of auxiliary voltage, the section of the sampling capacitor and the second controlled current source are connected to the array of redistribution and the control input of the second controlled current source is connected to the output controlling the second current source.

5 The one end of the second current source is connected to the source rail and the other end of the second current source is connected to the destination rail. The voltage supply is connected to the one end of the first current source whose control input is connected to the output controlling the first current source. The array of redistribution comprises the sections whose number equals the number of bits in the digital word. The section of the sampling capacitor and each section of the array of redistribution

10 comprises the source on-off switch, the destination on-off switch, the ground change-over switch and at least one capacitor. The top plate of the sampling capacitor and the top plate of each capacitor in the array of redistribution is connected through the source on-off switch to the source rail and/or to the destination rail through the destination on-off switch and the bottom plate is connected through the ground change-over switch to ground of the circuit or to the source of auxiliary voltage. In the array of redistribution, a capacitance value of each

15 capacitor of a given index is twice as high as a capacitance value of a capacitor of the previous index. The destination rail is connected through the destination rail on-off switch to ground of the circuit and is also connected to the non-inverting input of the second comparator whose inverting input is connected to the source of the reference voltage. The source rail is connected to the inverting input of the first comparator whose non-inverting input is connected to the source of auxiliary voltage. The control inputs of the source on-off switches and the

20 control input of the destination rail on-off switch are connected appropriately to control outputs of the control module. The control inputs of destination on-off switches and the control inputs of the ground change-over switches are coupled together and connected appropriately to the control outputs of the control module.

[0013] A significant innovation of the apparatus is that the other end of the first current source is connected to the section of the sampling capacitor comprising the additional sampling capacitor, the top plate change-over switches. The top plate of the sampling capacitor and the top plate

25 of the additional sampling capacitor are connected to the source on-off switch and to the destination on-off switch or to the other end of the first current source through the top plate change-over switches. The bottom plate of the sampling capacitor and the bottom plate of the additional sampling capacitor are connected to the ground change-over switch or to ground of the circuit through the bottom

plate change-over switches. The control inputs of the top plate change-over switches and the control inputs of the bottom plate change-over switches are coupled together and connected to the output controlling change-over switches of the plates.

[0014] It is advantageous if at least one section of the array of redistribution comprises the additional capacitor and the top plate change-over switches and the bottom plate change-over switches. The top plate of the capacitor and the top plates of the additional capacitor of such section are connected to the source on-off switch and to the destination on-off switch or to the other end of the first current source through the top plate change-over switches. The bottom plate of the capacitor and the bottom plate of the additional capacitor of such section are connected to the ground change-over switch or to ground of the circuit through the bottom plate change-over switches. The control inputs of the change-over top plate switches and the control inputs of bottom plate change-over switches are coupled together and connected to the output controlling change-over switches of the plates.

[0015] It is advantageous if the capacitance values of the sampling capacitor and of the additional sampling capacitor are not smaller than the capacitance value of the capacitor having the highest capacitance value in the array of redistribution.

[0016] It is also advantageous if the capacitance value of the additional capacitor in the array of redistribution equals appropriately the capacitance value of the capacitor in the array of redistribution.

[0017] Due to the accumulation of a portion of charge representing the next converted time interval in the additional sampling capacitor, it is possible to realize a conversion of two successive time intervals without a need to introduce a break to realize the process of redistribution of a portion of charge representing the previous time interval and to realize the relaxation phase. The accumulation of a portion of electric charge representing the next converted time interval in the additional sampling capacitor is realized simultaneously to the process of redistribution of the portion of charge representing the previous time interval and accumulated previously in the sampling capacitor.

[0018] In this way, the results of each conversion are presented with minimal delay equal to the time of realization of the process of charge redistribution. Moreover, the realization of actions related to the conversions of both time intervals by the same control module, by the array of redistribution, by the set of comparators and by the set the current sources contributes to a reduction of amount of energy consumed per single conversion by the apparatus and in this way increases energy efficiency of its operation. A start of a new conversion cycle after the detection of the end of the actual time interval enables the conversion of two successive time intervals by means of a single apparatus.

[0019] A use of a parallel connection of the additional capacitor having the highest capacitance value in the ar-

ray of redistribution to the additional sampling capacitor allows the required capacitance value of the sampling capacitor to be reduced twice and enables a significant reduction of area occupied by a converter produced in a form of the monolithic integrated circuit. Due to a parallel connection of the additional sampling capacitor to the additional capacitor having the highest capacitance value in the array of redistribution, the maximum voltage value created on the additional sampling capacitor having the reduced capacitance value is not increased. Furthermore the time of realization of redistribution of charge, accumulated in the additional sampling capacitor and in the additional capacitor having the highest capacitance value in the array of redistribution connected to the additional sampling capacitor in parallel, is smaller at least by 25%.

[0020] Conserving in the apparatus a small portion of charge which has not been taken into consideration in the value of a digital word is also an advantage. The inclusion of the abovementioned portion of charge during the process of redistribution of the subsequent accumulated charge portion together with elimination of the need to introduce breaks between consecutive conversions causes that the sum of digital words representing a sequence of converted time intervals with the resolution defined by the quantization error.

[0021] The subject of the invention is explained in the exemplary realizations by means of figures where the apparatus is shown at different phases of conversion process represented by different states of on-off switches and change-over switches:

Fig. 1 illustrates the schematic diagram of the apparatus in the phase of relaxation before the beginning of the conversion process.

Fig. 2 illustrates the schematic diagram of the apparatus during accumulation of electric charge in the sampling capacitor C_n .

Fig. 3 illustrates the schematic diagram at the beginning of redistribution of charge accumulated in the sampling capacitor C_n .

Fig. 4 illustrates exemplary sequence of converted time intervals.

Fig. 5 illustrates exemplary sequence of converted time intervals which occur immediately after themselves.

Fig. 6 illustrates the schematic diagram of the apparatus during the charge transfer from the source capacitor C_i to the destination capacitor C_k .

Fig. 7 illustrates the schematic diagram at the beginning of redistribution of charge accumulated in the additional sampling capacitor C_{nA} .

Fig. 8 illustrates the schematic diagram of the apparatus in the phase of relaxation before the beginning of the conversion process.

Fig. 9 illustrates the schematic diagram during accumulation of charge in the sampling capacitor C_n and in the capacitor C_{n-1} which is connected to the sampling capacitor C_n in parallel.

Fig. 10 illustrates the schematic diagram at the beginning of redistribution of charge accumulated in the sampling capacitor C_n and in the capacitor C_{n-1} .

Fig. 11 illustrates the schematic diagram at the beginning of redistribution of charge accumulated in the additional sampling capacitor C_{nA} and in the additional capacitor C_{n-1A} . According to the invention, the method for clockless conversion of a time interval to a digital word consists in that the beginning and the end of the time interval T_x are detected by the use of the control module CM and this time interval is mapped by a portion of electric charge which is proportional to that converted time interval. Electric charge is delivered by the use of the first current source I during the time interval T_x and accumulated in the sampling capacitor C_n . Then, the process of redistribution of the accumulated charge is realized in the array of redistribution A by means of the control module CM by changing the states of the signals from the relevant control outputs and the relevant values are assigned to the bits $b_{n-1}, b_{n-2}, \dots, b_1, b_0$ in digital word by means of the control module CM. The array of redistribution A comprises the set of on-off switches, the set of change-over switches and the set of capacitors while a capacitance value of a capacitor of a given index is twice as high as a capacitance value of a capacitor of the previous index.

[0022] As soon as accumulation of charge in the sampling capacitor C_n is terminated and when the beginning of next time interval T_{x+1} is detected by means of the control module CM, the charge is delivered by the use of the first current source I and accumulated in the additional sampling capacitor C_{nA} . Next, the process of redistribution of charge accumulated in the additional sampling capacitor C_{nA} is realized and the relevant values are assigned to the bits $b_{n-1}, b_{n-2}, \dots, b_1, b_0$ in the digital word by means of the control module CM. The accumulation of charge in the additional sampling capacitor C_{nA} , the process of redistribution of charge accumulated in the additional sampling capacitor C_{nA} and the assignment of relevant values to the bits $b_{n-1}, b_{n-2}, \dots, b_1, b_0$ in the digital word are realized in the same way as for the sampling capacitor C_n .

[0023] The another exemplary solution is characterized in that as soon as accumulation of electric charge in the additional sampling capacitor C_{nA} is terminated and when the beginning of the subsequent time interval

T_{x+2} is detected by means of the control module CM, the next cycle begins and the charge is delivered by the use of the first current source I and accumulated in the sampling capacitor C_n again.

[0024] The another exemplary solution is characterized in that during the next time interval T_{x+1} when the charge is delivered by the use of the first current source I and accumulated in the additional sampling capacitor C_{nA} , a part of delivered charge is accumulated simultaneously in the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution which is connected to the additional sampling capacitor C_{nA} in parallel. The capacitance value of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution is equal to the capacitance value of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution.

[0025] The another exemplary solution is characterized in that as soon as the process of redistribution is terminated in the last of capacitors on which reference voltage U_L had not been reached when the process of redistribution is realized, the charge accumulated in the last of capacitors is conserved.

[0026] In detail, the abovementioned process of redistribution in the exemplary solution is presented as follows.

[0027] As soon as accumulation of electric charge in the sampling capacitor C_n is terminated, the function of the source capacitor C_i , whose index is defined by the content of the source index register, is assigned by means of the control module CM to the sampling capacitor C_n by writing the value of the index of the sampling capacitor C_n to this register. Simultaneously, the function of the destination capacitor C_k , whose index is defined by the content of the destination index register, is assigned by means of the control module CM to the capacitor C_{n-1} having the highest capacitance value in the array of redistribution by writing the value of the index of the capacitor C_{n-1} to this register. Then, the process of redistribution of the accumulated charge is realized by transfer of the charge from the source capacitor C_i to the destination capacitor C_k by the use of the second current source J having the effectiveness twice as high as the effectiveness of the first current source I.

[0028] At the same time, the voltage U_k increasing on the destination capacitor C_k is compared to the reference voltage U_L by the use of the second comparator K2, and also the voltage U_i on the source capacitor C_i is observed by the use of the first comparator K1.

[0029] When the voltage U_i on the source capacitor C_i observed by the use of the first comparator K1 equals zero during the charge transfer, the function of the source capacitor C_i is assigned to the current destination capacitor C_k by means of the control module CM on the basis of the output signal of the first comparator K1 by writing the current content of the destination index register to the source index register, and the function of the destination capacitor C_k is assigned to the subsequent capac-

itor in the array of redistribution A whose capacitance value is twice lower than the capacitance value of the capacitor that acted as the destination capacitor directly before by reducing the content of the destination index register by one, and the charge transfer from a new source capacitor C_i to a new destination capacitor C_k is continued by the use of the second current source J.

[0030] When the voltage U_k on the destination capacitor C_k observed by the use of the second comparator K2 equals the reference voltage U_L during the transfer of charge from the source capacitor C_i to the destination capacitor C_k , the function of the destination capacitor C_k is assigned by means of the control module CM on the basis of the output signal of the second comparator K2 to the subsequent capacitor in the array of redistribution A whose capacitance value is twice lower than the capacitance value of the capacitor that acted as the destination capacitor directly before by reducing the content of the destination index register by one, and also the charge transfer from the source capacitor C_i to a new destination capacitor C_k is continued.

[0031] The process of redistribution is still controlled by means of the control module CM on the basis of the output signals of both comparators (K1 and K2) until the voltage U_i on the source capacitor C_i observed by the use of the first comparator K1 equals zero during the period of time when the function of the destination capacitor C_k is assigned to the capacitor C_0 having the lowest capacitance value in the array of redistribution, or the voltage U_0 increasing on the capacitor C_0 having the lowest capacitance value in the array of redistribution and observed at the same time by the use of the second comparator K2 equals the reference voltage U_L . The value one is assigned to the bits in the digital word corresponding to the capacitors in the array of redistribution on which the voltage equal to the reference voltage value U_L has been obtained, and the value zero is assigned to the other bits by means of the control module CM.

[0032] According to the invention, the apparatus for clockless conversion of the time interval to the digital word comprises the array of redistribution A whose control inputs are connected to control outputs of the control module CM. The control module CM is equipped with the digital output B, the complete conversion output OutR, the time interval signal input InT, the first control input In1 connected to the output of the first comparator K1 and the other control input In2 connected to the output of the second comparator K2. The source of auxiliary voltage U_H , the section of the sampling capacitor A_n and the second controlled current source J having the effectiveness twice as high as the effectiveness of the first current source I are connected to the array of redistribution A. The control input of the second current source J is connected to the output controlling the current source A_j . The one end of the second current source J is connected to the source rail H and the other end of the second current source J is connected to the destination rail L. The voltage supply U_{DD} is connected to the one end of

the first current source I whose control input is connected to the output controlling the first current source A_i .

[0033] The array of redistribution comprises the sections whose number n equals the number of bits in the digital word. The section of the sampling capacitor A_n and the sections of the array of redistribution A comprise the source on-off switches $S_{Hn}; S_{Hn-1}, S_{Hn-2}, \dots, S_{H1}, S_{H0}$, the destination on-off switches $S_{Ln}; S_{Ln-1}, S_{Ln-2}, \dots, S_{L1}, S_{L0}$, the ground change-over switches $S_{Gn}; S_{Gn-1}, S_{Gn-2}, \dots, S_{G1}, S_{G0}$ and the capacitors $C_n; C_{n-1}, C_{n-2}, \dots, C_1, C_0$. The top plates of the capacitors $C_{n-1}, C_{n-2}, \dots, C_1, C_0$ of the array of redistribution are connected to the source rail H through the source on-off switches $S_{Hn-1}, S_{Hn-2}, \dots, S_{H1}, S_{H0}$ and to the destination rail L through the destination on-off switches $S_{Ln-1}, S_{Ln-2}, \dots, S_{L1}, S_{L0}$. The bottom plates of these capacitors are connected to ground of the circuit and to the source of auxiliary voltage U_H through the ground change-over switches $S_{Gn-1}, S_{Gn-2}, \dots, S_{G1}, S_{G0}$. In the array of redistribution A, a capacitance value of each capacitor $C_{n-1}, C_{n-2}, \dots, C_1, C_0$ of a given index is twice as high as a capacitance value of a capacitor of the previous index. The capacitance value of the sampling capacitor C_n is twice as high as the capacitance value of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution. The relevant bit $b_{n-1}, b_{n-2}, \dots, b_1, b_0$ in the digital word is assigned to each capacitor $C_{n-1}, C_{n-2}, \dots, C_1, C_0$ in the array of redistribution. The destination rail L is connected through the destination rail on-off switch S_{Gal} to ground of the circuit and is also connected to the non-inverting input of the second comparator K2 whose inverting input is connected to the source of the reference voltage U_L . The source rail H is connected to the inverting input of the first comparator K1 whose non-inverting input is connected to the source of auxiliary voltage U_H . The control inputs of the source on-off switches $S_{Hn}; S_{Hn-1}, S_{Hn-2}, \dots, S_{H1}, S_{H0}$ and the control inputs of the destination rail on-off switch S_{Gal} are connected appropriately to the control outputs $D_n; D_{n-1}, D_{n-2}, \dots, D_1, D_0; D_{all}$. The control inputs of the destination on-off switches $S_{Ln}; S_{Ln-1}, S_{Ln-2}, \dots, S_{L1}, S_{L0}$ and the control inputs of the ground change-over switches $S_{Gn}; S_{Gn-1}, S_{Gn-2}, \dots, S_{G1}, S_{G0}$ are coupled together and connected appropriately to the control outputs $I_n; I_{n-1}, I_{n-2}, \dots, I_1, I_0$.

[0034] The other end of the first current source I is connected to the section of the sampling capacitor A_n comprising the additional sampling capacitor C_{nA} , the top plate change-over switches S_{Tn}, S_{TnA} and the bottom plate change-over switches S_{Bn}, S_{BnA} . The capacitance value of the additional sampling capacitor C_{nA} is equal to the capacitance value of the sampling capacitor C_n . The top plate of the sampling capacitor C_n and the top plate of the additional sampling capacitor C_{nA} are connected to the source on-off switch S_{Hn} , to the destination on-off switch S_{Ln} and to the other end of the first current source I through the top plate change-over switches S_{Tn}, S_{TnA} . The bottom plates of the sampling capacitor C_n and the bottom plates of the additional sampling capac-

itor C_{nA} are connected to the ground change-over switch S_{Gn} and to ground of the circuit through the bottom plate change-over switches S_{Bn} , S_{BnA} . The control inputs of the top plate change-over switches S_{Tn} , S_{TnA} and the control inputs of the bottom plate change-over switches S_{Bn} , S_{BnA} are coupled together and connected to the output controlling the change-over switches of the plates A_C . The source on-off switch S_{Hn} is connected to the source rail H, the destination on-off switch S_{Ln} is connected to the destination rail L and the ground change-over switch S_{Gn} is connected to ground of the circuit and to the source of auxiliary voltage U_H .

[0035] In the another exemplary solution, the section of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution comprises the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution, the top plate change-over switches S_{Tn-1} , S_{Tn-1A} and the bottom plate change-over switches S_{Bn-1} , S_{Bn-1A} . The capacitance value of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution is equal to the capacitance value of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution. The top plates of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution and the top plates of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution are connected to the source on-off switch S_{Hn-1} , to the destination on-off switch S_{Ln-1} and to the other end of the first current source I through the top plate change-over switches S_{Tn-1} , S_{Tn-1A} . The bottom plates of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution and the top plates of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution are connected to the ground change-over switch S_{Gn-1} and to ground of the circuit through the bottom plate change-over switches S_{Bn-1} , S_{Bn-1A} . The control inputs of the top plate change-over switches S_{Tn-1} , S_{Tn-1A} and the control inputs of the bottom plate change-over switches S_{Bn-1} , S_{Bn-1A} are coupled together and connected to the output controlling the change-over switches of the plates A_C .

[0036] The method for conversion of a time interval to the digital word, according to the invention, is presented in the first exemplary apparatus as follows. Before the first process of conversion of a time interval to the digital word having the number of bits equal to n, the control module CM introduces the complete conversion output OutR to the inactive state. The control module CM by the use of the signal from the output controlling the first current source A_I causes the switching off the first current source I and by the use of the signal from the output controlling the second current source A_J causes the switching off the second current source J. By the use of the signal from the output controlling the change-over switches of the plates A_C , the control module CM causes the switching of the top plate change-over switches S_{Tn} , S_{TnA} and of the bottom plate change-over switches S_{Bn} ,

S_{BnA} and the connection of the top plate of the sampling capacitor C_n to the source on-off switch S_{Hn} and to the destination on-off switch S_{Ln} , the connection of the top plate of the additional sampling capacitor C_{nA} to the other end of the first current source I, the connection of the bottom plate of the sampling capacitor C_n to the ground change-over switch S_{Gn} and the connection of the bottom plate of the additional sampling capacitor C_{nA} to ground of the circuit. Next, the control module CM introduces the apparatus into the relaxation state shown in fig.1. Therefore, the control module CM causes the opening of the source on-off switches S_{Hn-1} , S_{Hn-2} , ..., S_{H1} , S_{H0} by the use of the signals from the control outputs D_{n-1} , D_{n-2} , ..., D_1 , D_0 . Furthermore, by the use of the signals from the control outputs I_n , I_{n-1} , I_{n-2} , ..., I_1 , I_0 , the control module CM causes the closure of the destination on-off switches S_{Ln} , S_{Ln-1} , S_{Ln-2} , ..., S_{L1} , S_{L0} and the connection of the top plate of the sampling capacitor C_n and the top plates of all the capacitors C_{n-1} , C_{n-2} , ..., C_1 , C_0 in the array of redistribution to the destination rail L, the switching of the ground change-over switches S_{Gn} , S_{Gn-1} , S_{Gn-2} , ..., S_{G1} , S_{G0} and the connection of the bottom plate of the sampling capacitor C_n and the bottom plates of all the capacitors C_{n-1} , C_{n-2} , ..., C_1 , C_0 in the array of redistribution to ground of the circuit. By the use of the signal from the control output D_{all} , the control module CM causes the closure of the destination rail on-off switch S_{Gal} and the connection of the destination rail L to ground of the circuit enforcing a complete discharge of the sampling capacitor C_n and of all the capacitors C_{n-1} , C_{n-2} , ..., C_1 , C_0 in the array of redistribution. At the same time, by the use of signal from the control output D_n , the control module CM causes the closure of the source on-off switch S_{Hn} and the connection of the source rail H to the destination rail L and to ground of the circuit which prevents the occurrence of a random potential on the source rail H.

[0037] As soon as the beginning of the time interval T_x is detected on the time interval signal input InT by the module CM, the apparatus is introduced into the state shown in fig. 2 by the use of the module CM. Therefore, by the use of the signal from the output controlling the change-over switches of the plates A_C , the control module CM causes the switching of the top plate change-over switches S_{Tn} , S_{TnA} and switching of the bottom plate change-over switches S_{Bn} , S_{BnA} and the connection of the top plate of the sampling capacitor C_n to the other end of the first current source I, the connection of the top plate of the additional sampling capacitor C_{nA} to the source on-off switch S_{Hn} and to the destination on-off switch S_{Ln} , the connection of the bottom plate of the sampling capacitor C_n to ground of the circuit and the connection of the bottom plate of the additional sampling capacitor C_{nA} to the ground change-over switch S_{Gn} enforcing a complete discharge of the additional sampling capacitor C_{nA} . Next, the control module CM by the use of the signal from the output controlling the first current source A_I causes the switching on the first current source I. Electric charge delivered by the use of the first current

source I is accumulated in the sampling capacitor C_n which as the only capacitor is then connected to the other end of the first current source I through the top plate change-over switch S_{Tn} .

[0038] As soon as the end of the time interval T_x is detected by the control module CM on the time interval signal input Int, the control module CM introduces the apparatus into the state shown in fig. 3. Therefore, by the use of the signal from the control output D_{all} , the control module CM causes the opening of the destination rail on-off switch S_{Gal} and the disconnection of the destination rail L from ground of the circuit. By the use of the signals from control outputs $I_n; I_{n-2}, \dots, I_1, I_0$, the control module CM causes the opening of the destination on-off switches $S_{Ln}; S_{Ln-2}, \dots, S_{L1}, S_{L0}$ and the disconnection of the top plate of the additional sampling capacitor C_{nA} and the top plates of the capacitors C_{n-2}, \dots, C_1, C_0 in the array of redistribution from the destination rail L, the switching of the ground change-over switches $S_{Gn}; S_{Gn-2}, \dots, S_{G1}, S_{G0}$ and the connection of the bottom plate of the additional sampling capacitor C_{nA} and the bottom plates of the capacitors C_{n-2}, \dots, C_1, C_0 in the array of redistribution to the source of auxiliary voltage U_H . By the use of the signal from the output controlling the change-over switches of the plates A_C , the control module CM causes the switching of the top plate change-over switches S_{Tn}, S_{TnA} and of the bottom plate change-over switches S_{Bn}, S_{BnA} and the connection of the top plate of the sampling capacitor C_n to the source on-off switch S_{Hn} and to the destination on-off switch S_{Ln} , the connection of the top plate of the additional sampling capacitor C_{nA} to the other end of the first current source I, the connection of the bottom plate of the sampling capacitor C_n to the ground change-over switch S_{Gn} and the connection of the bottom plate of the additional sampling capacitor C_{nA} to ground of the circuit.

[0039] If the end of the time interval T_x detected by the control module CM does not constitute the beginning of the next time interval T_{x+1} as it is shown in fig. 4, the control module CM by the use of the signal from the output controlling the first current source A_I causes the switching off of the first current source I.

[0040] As soon as the beginning of the next time interval T_{x+1} is detected by the control module CM on the time interval signal input Int, the control module CM by the use of the signal from the output controlling the first current source A_I causes again the switching on the first current source I. The charge is delivered by the use of the first current source I and accumulated in the additional sampling capacitor C_{nA} which as the only capacitor is then connected to the other end of the first current source I through the top plate change-over switch S_{TnA} .

[0041] If the end of the time interval T_x detected by the control module CM determines simultaneously the beginning of the next time interval T_{x+1} as it is shown in fig. 5, the charge delivered still by the use of the first current source I is accumulated in the additional sampling capacitor C_{nA} which as the only capacitor is then connected

the other end of the first current source I through the top plate change-over switch S_{TnA} .

[0042] In both cases, the control module CM introduces the complete conversion output OutR into the inactive state and assigns the initial value zero to all the bits $b_{n-1}, b_{n-2}, \dots, b_1, b_0$ in the digital word. Then, the control module CM assigns the function of the source capacitor C_i to the sampling capacitor C_n by writing the value of the index of the sampling capacitor to the source index register. Simultaneously, the control module CM assigns the function of the destination capacitor C_k to the capacitor C_{n-1} having the highest capacitance value in the array of redistribution by writing the value of the index of the capacitor having the highest capacitance value in the array of redistribution to the destination index register. Next, the control module CM starts to realize the process of redistribution of the accumulated electric charge. Therefore, the control module CM by the use of the signal from the output controlling the second current source A_J causes the switching on the second current source J. The charge accumulated in the source capacitor C_i is transferred to the destination capacitor C_k by the use of the second current source J though the source rail H and though the destination rail L and the voltage U_i on the source capacitor gradually decreases and at the same time the voltage U_k on the destination capacitor gradually increases during the charge transfer.

[0043] In case when the voltage U_k on the current destination capacitor C_k reaches the reference voltage U_L value, then the value one is assigned by the control module CM to the appropriate bit b_k in the digital word on the basis of the output signal of the second comparator K2. By the use of the signal from the control output I_k , the control module CM causes the opening of the destination on-off switch S_{Lk} and the disconnection of the top plate of the destination capacitor C_k from the destination rail L, the simultaneous switching of the ground change-over switch S_{Gk} and the connection of the bottom plate of the destination capacitor C_k to the source of auxiliary voltage U_H . Next, the control module CM assigns the function of the destination capacitor C_k to the subsequent capacitor in the array of redistribution A whose capacitance value is twice lower than the capacitance value of the capacitor that acted as the destination comparator C_k directly before by reducing the content of the destination index register by one. By the use of the signal from the control output I_k , the control module CM causes the closure of the destination on-off switch S_{Lk} and the connection of the top plate of a new destination capacitor C_k to the destination rail L, the simultaneous switching of the ground change-over switch S_{Gk} and the connection of the bottom plate of the destination capacitor C_k to ground of the circuit.

[0044] In case when the voltage U_i on the source capacitor reaches the value zero during charge transfer, then the control module CM on the basis of the output signal of the first comparator K1 by the use of the signal from the control output D_i causes the opening of the

source on-off switch S_{Hi} and the disconnection of the top plate of the source capacitor C_i from the source rail H. By the use of the signal from the control output I_k , the control module CM causes the opening of the destination on-off switch S_{Lk} and the disconnection of the top plate of the destination capacitor C_k from the destination rail L, the simultaneous switching of the ground change-over switch S_{Gk} and the connection of the bottom plate of the destination capacitor C_k to the source of auxiliary voltage U_H . Next, the function of the source capacitor C_i is assigned by the control module CM to the capacitor that acted as the destination capacitor C_k directly before by writing the current content of the destination index register to the source index register. The control module CM by the use of the signal from the control output D_i causes the closure of the source on-off switch S_{Hi} and the connection of the top plate of a new source capacitor C_i to the source rail H. Then, the control module CM reduces the content of the destination index register by one and assigns the function of the destination capacitor C_k to the next capacitor in the array of redistribution A having a capacitance value twice lower than the capacitance value of the capacitor that acted as the destination capacitor C_k directly before. By the use of the signal from the control output I_k , the control module CM causes the closure of the destination on-off switch S_{Lk} and the connection of the top plate of a new destination capacitor C_k to the destination rail L, the simultaneous switching of the ground change-over switch S_{Gk} and the connection of the bottom plate of a new destination capacitor C_k to ground of the circuit. Fig. 6 presents the apparatus in the abovementioned state.

[0045] In both abovementioned cases, the control module CM continues the process of electric charge redistribution on the basis of the output signals of the first comparator K1 and of the second comparator K2. Each occurrence of the active state on the output of the second comparator K2 causes the assignment of the function of the destination capacitor C_k to the subsequent capacitor in the array of redistribution A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor C_k directly before. On the other hand, each occurrence of the active state on the output of first comparator K1 causes the assignment of the function of the source capacitor C_i to the capacitor in the array of redistribution A that until now has acted as the destination capacitor C_k , and at the same time the assignment of the function of the destination capacitor C_k to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before. The process of redistribution is terminated when the capacitor C_0 having the lowest capacitance value in the array of redistribution A stops to act as the destination capacitor C_k . Such situation occurs when the active state appears on the output of the first comparator K1 or on the output of the second comparator K2 during charge transfer to the capacitor

C_0 having the lowest capacitance value in the array of redistribution A. When the active state appears on the output of the second comparator K2, the control module CM assigns the value one to the bit b_0 . After termination

- 5 of redistribution of charge accumulated previously in the sampling capacitor C_n and after assigning the corresponding values to the bits $b_{n-1}, b_{n-2}, \dots, b_1, b_0$ in the output digital word, the control module CM activates the signal provided on the complete conversion signal output
- 10 OutR. By the use of the signal from the output controlling the second current source A_j , the control module CM causes the switching off the second current source J. Next, the control module CM introduces the apparatus into the relaxation phase shown in fig. 1.
- 15 **[0046]** After detecting the end of the next time interval T_{x+1} by the control module CM on the time interval signal input InT, the control module CM introduces the apparatus into the state shown in fig. 7. Therefore, the control module CM by the use of the signal from the control output
- 20 D_{all} causes the opening of the destination rail on-off switch S_{Gal} and the disconnection of the destination rail L from ground of the circuit. The control module CM by the use of signals from the control outputs $I_n; I_{n-2}, \dots, I_1, I_0$ causes the opening of the destination on-off switches $S_{Ln}; S_{Ln-2}, \dots, S_{L1}, S_{L0}$ and the disconnection of the top plates of the sampling capacitor C_n and of the capacitors C_{n-2}, \dots, C_1, C_0 in the array of redistribution from the destination rail L, the switching of the ground change-over switches $S_{Gn}; S_{Gn-2}, \dots, S_{G1}, S_{G0}$ and the connection of
- 25 the bottom plate of the sampling capacitor C_n and the bottom plates of the capacitors C_{n-2}, \dots, C_1, C_0 in the array of redistribution to the source of auxiliary voltage U_H . By the use of the signal from the output controlling change-over switches of the plates A_C , the control module
- 30 CM causes the switching of the top plate change-over switches S_{Tn}, S_{TnA} and of the bottom plate change-over switches S_{Bn}, S_{BnA} and the connection of the top plate of the sampling capacitor C_n to the other end of the first current source I, the connection of the top plate of the additional sampling capacitor C_{nA} to the source on-off switch S_{Hn} and to the destination on-off switch S_{Ln} , the connection of the bottom plate of the sampling capacitor C_n to ground of the circuit and the connection of the bottom plate of the additional sampling capacitor C_{nA} to the ground change-over switch S_{Gn} .

- 45 **[0047]** In case when the end of the time interval T_{x+1} detected by the control module CM does not constitute simultaneously the beginning of the subsequent time interval T_{x+2} as it is shown in fig. 4, the control module CM by the use of the signal from the output controlling the first current source A_i causes the switching off the first current source I. As soon as the beginning of the subsequent time interval T_{x+2} is detected by the control module CM on the time interval signal input InT, the control module CM by the use of the signal from the output controlling the first current source A_i causes again the switching on the first current source I. The charge delivered by the use of the first current source I is accumulated in the sampling

capacitor C_n which is then the only capacitor connected to the other end of the first current source I through the top plate change-over switch S_{Tn} .

[0048] In case when the end of the next time interval T_{x+1} detected by the control module CM constitutes simultaneously the beginning of the subsequent trigger signal T_{x+2} as it is shown in fig. 5, electric charge delivered by the use of the first current source I is accumulated in the sampling capacitor C_n which is then the only capacitor connected to the other end of the first current source I through the top plate change-over switch S_{Tn} .

[0049] In both cases, the control module CM deactivates the signal provided on the complete conversion signal output OutR and assigns the initial value zero to all the bits $b_{n-1}, b_{n-2}, \dots, b_1, b_0$ in the digital word. Then, the control module CM assigns the function of the source capacitor C_i to the additional sampling capacitor C_{nA} by writing the value of the sampling capacitor C_n index to the source index register. Simultaneously, the control module CM assigns the function of the destination capacitor C_k to the capacitor C_{n-1} having the highest capacitance value in the array of redistribution by writing a value of the index of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution to the destination index register. Next, the control module CM by the use of the signal from the output controlling the second current source A_j causes the switching on the second current source J and starts to realize the process of redistribution of charge accumulated in the additional sampling capacitor C_{nA} . The process of redistribution is terminated when the capacitor C_0 having the lowest capacitance value in the array of redistribution A stops to act as the destination capacitor C_k .

[0050] After termination of redistribution of charge accumulated previously in the additional sampling capacitor C_{nA} and after assigning the corresponding values to the bits $b_{n-1}, b_{n-2}, \dots, b_1, b_0$ in the digital word, the control module CM activates the complete conversion signal output OutR. By the use of the signal from the output controlling the second current source A_j , the control module CM causes the switching off the current source J. Next, the control module CM introduces the apparatus into the relaxation phase shown in fig. 2.

[0051] The method for conversion of a time interval to the digital word, according to the invention, is presented in the second exemplary apparatus as follows.

Before the start of the first process of conversion of a time interval to the digital word having the number of bits equal to n, the control module CM by the use of the signal from the output controlling the change-over switches of plates A_C causes additionally the switching of top plate change-over switches S_{Tn-1}, S_{Tn-1A} and switching of the bottom plate change-over switches S_{Bn-1}, S_{Bn-1A} and the connection of the top plate of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution to the source on-off switch S_{Hn-1} and to the destination on-off switch S_{Ln-1} , the connection of the top plate of the additional capacitor C_{n-1A} having the highest ca-

pacitance value in the array of redistribution to the other end of the first current source I, the connection of the bottom plate of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution to the ground change-over switch S_{Gn-1} and the connection of the bottom plate of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution to ground of the circuit. Fig. 8 presents the abovementioned state of the apparatus.

[0052] As soon as the beginning of the time interval T_x is detected by the control module CM on the time interval signal input InT, the control module CM by the use of the signal from the output controlling the change-over switches of the plates A_C causes additionally the switching of the top plate change-over switches S_{Tn-1}, S_{Tn-1A} and switching of the bottom plate change-over switches S_{Bn-1}, S_{Bn-1A} and the connection of the top plate of the sampling capacitor C_{n-1} having the highest capacitance value in the array of redistribution to the other end of the first current source I, the connection of the top plate of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution to the source on-off switch S_{Hn-1} and to the destination on-off switch S_{Ln-1} , the connection of the bottom plate of the sampling capacitor C_{n-1} having the highest capacitance value in the array of redistribution to ground of the circuit and the connection of the bottom plate of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution to the ground change-over switch S_{Gn-1} enforcing a complete discharge of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution. Electric charge delivered by the use of the first current source I is accumulated simultaneously in the sampling capacitor C_n and in the capacitor C_{n-1} having the highest capacitance value in the array of redistribution which is connected to the sampling capacitor C_n in parallel. Both capacitors (C_n and C_{n-1}) are the only capacitors that are connected to the other end of the first current source I through the top plate change-over switches S_{Tn}, S_{Tn-1} . Fig. 9 presents the abovementioned state of the apparatus.

[0053] After detecting the end of the time interval T_x by the control module CM on the time interval signal input InT, the control module CM by the use of the signal from the output controlling the change-over switches of plates A_C causes additionally switching of the top plate change-over switches S_{Tn-1}, S_{Tn-1A} and switching of the bottom plate change-over switches S_{Bn-1}, S_{Bn-1A} and the connection of the top plate of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution to the source on-off switch S_{Hn-1} and to the destination on-off switch S_{Ln-1} , the connection of the top plate of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution to the other end of the first current source I, the connection of the bottom plate of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution to the ground change-over switch S_{Gn} and the connection of the bottom plate

of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution to ground of the circuit. Fig. 10 presents the abovementioned state of the apparatus.

[0054] As soon as the beginning of the next time interval T_{x+1} is detected by the control module CM on the time interval signal input InT, the electric charge delivered by the use of the first current source I is accumulated simultaneously in the additional sampling capacitor C_{nA} and in the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution which is connected to the additional sampling capacitor C_{nA} in parallel. Both capacitors (C_{nA} and C_{n-1A}) are the only capacitors that are connected to the other end of the first current source I through the top plate change-over switches S_{TnA} , S_{Tn-1A} .

[0055] After detecting the end of the next time interval T_{x+1} by the control module CM on the time interval signal input InT, the control module CM by the use of the signal from the output controlling the change-over switches of the plates A_C causes the switching of the top plate change-over switches S_{Tn-1} , S_{Tn-1A} and switching of the bottom plate change-over switches S_{Bn-1} , S_{Bn-1A} and the connection of the top plate of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution to the other end of the first current source I, the connection of the top plate of the additional capacitor C_{n-1A} having the highest capacitance value in the array of redistribution to the source on-off switch S_{Hn-1} and to the destination on-off switch S_{Ln-1} , the connection of the bottom plate of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution to ground of the circuit and the connection of the bottom plate of the additional capacitor C_{n-1A} to the ground change-over switch S_{Gn-1} . Fig. 11 presents the abovementioned state of the apparatus.

[0056] Another method for conversion of a time interval to the digital word, according to the invention, realized in the exemplary apparatus differs from the previous methods in that as soon as the process of accumulated electric charge redistribution is terminated, the control module CM causes the electric charge, accumulated in the last of capacitors on which the reference voltage U_L had not been reached during realization of the process of redistribution, to be conserved.

[0057] If the control module CM assigns the value zero to the bit b_0 during the realization of the process of charge redistribution, the control module CM introducing the apparatus into the relaxation state by the use of the signal from the control output I_0 causes the opening of the destination on-off switch S_{L0} and the disconnection of the top plate of the capacitor C_0 having the lowest capacitance value in the array of redistribution from the destination rail L, the switching of the ground change-over switch S_{G0} and the connection of the bottom plate of the capacitor C_0 having the lowest capacitance value in the array of redistribution to the source of auxiliary voltage U_H .

If the control module CM assigns the value one to the bit b_0 during the realization of the process of redistribution, the control module CM introducing the apparatus into relaxation state by the use of the signal from the control output I_1 causes the opening of the destination on-off switch S_{Li} and the disconnection of the top plate of the source capacitor C_i from the destination rail L, the switching of the ground change-over switch S_{Gi} and the connection of the bottom plate of the source capacitor C_i to the source of auxiliary voltage U_H .

References

[0058]

15 A array of redistribution

16 A_n section of sampling capacitor

20 CM control module

K1 first comparator

25 K2 second comparator

I first current source

J second current source

30 U_H source of auxiliary voltage

U_L source of the reference voltage

U_{DD} voltage supply

35 InT time interval signal input InT

In1 first control input of the control module

40 In2 second control input of the control module

B digital output of the control module

45 OutR complete conversion output

H source rail

L destination rail

50 C_n sampling capacitor

$C_{n-1}, C_{n-2}, \dots, C_1, C_0$ capacitors in the array of redistribution

55 C_{n-1} capacitor having the highest capacitance value in the array of redistribution

C_0 capacitor having the lowest capacitance value in

the array of redistribution	Claims
C_{nA} additional sampling capacitor	
C_{n-1A} additional capacitor having the highest capacitance value in the array of redistribution	5
C_i source capacitor	
C_k destination capacitor	10
$U_{n-1}, U_{n-2}, \dots, U_1, U_0$ voltages on the capacitors in the array of redistribution	
U_i voltage on the source capacitor	15
U_k voltage on the destination capacitor	
$b_{n-1}, b_{n-2}, \dots, b_i, \dots, b_k, \dots, b_1, b_0$ bits in the digital word	20
$S_{Hn}, S_{Hn-1}, S_{Hn-2}, \dots, S_{Hi}, \dots, S_{Hk}, \dots, S_{H1}, S_{H0}$ source on-off switches	
$S_{Ln}, S_{Ln-1}, S_{Ln-2}, \dots, S_{Li}, \dots, S_{Lk}, \dots, S_{L1}, S_{L0}$ destination on-off switches	25
$S_{Gn}, S_{Gn-1}, S_{Gn-2}, \dots, S_{Gi}, \dots, S_{Gk}, \dots, S_{G1}, S_{G0}$ ground change-over switches	
$S_{Tn}, S_{Tn-1}, S_{TnA}, S_{Tn-1A}$ top plate change-over switches	30
$S_{Bn}, S_{Bn-1}, S_{BnA}, S_{Bn-1A}$ bottom plate change-over switches	35
S_{Gal} destination rail on-off switch	
A_C output controlling change-over switches of the plates	40
A_i output controlling the first current source	
A_j output controlling the second current source	
T_x time interval	45
T_{x+1} next time interval	
T_{x+2} subsequent time interval	50
$I_n, I_{n-1}, I_{n-2}, \dots, I_i, \dots, I_k, \dots, I_1, I_0$ control outputs	
$D_n, D_{n-1}, D_{n-2}, \dots, D_i, \dots, D_k, \dots, D_1, D_0, D_{all}$ control outputs	55
	<p>1. Method for clockless conversion of time interval to digital word consisting in a detection of the beginning and of the end of the time interval by the use of a control module and in mapping this time interval to a portion of electric charge proportional to this time interval and delivered by the use of a current source while the portion of electric charge is accumulated in a sampling capacitor, or in the sampling capacitor and in the capacitor having the highest capacitance value in an array of redistribution, which is connected to the sampling capacitor in parallel, and then consisting in the realization of the process of accumulated electric charge redistribution in the array of redistribution by means of the control module by changes of states of signals from relevant control outputs, while the array of redistribution comprises an array of on-off switches, of change-over switches and of capacitors such that a capacitance value of each capacitor of a given index is twice as high as a capacitance value of a capacitor of the previous index, and also consisting in the assignment of relevant values to bits of the digital word by means of the control module characterized in that after termination of accumulation of electric charge in the sampling capacitor (C_n), or in the sampling capacitor (C_n) and in the capacitor (C_{n-1}) having the highest capacitance value in the array of redistribution which is connected to the sampling capacitor (C_n) in parallel, and after detection of the beginning of a next time interval (T_{x+1}) by means of the control module (CM), electric charge is delivered by the use of the current source and accumulated in an additional sampling capacitor (C_{nA}), and next the process of redistribution of electric charge accumulated in the additional sampling capacitor (C_{nA}) is realized and relevant values are assigned to bits ($b_{n-1}, b_{n-2}, \dots, b_1, b_0$) in the digital word by means of the control module (CM) while accumulation of electric charge in the additional sampling capacitor (C_{nA}) and the process of redistribution of electric charge accumulated in the additional sampling capacitor (C_{nA}) and assignment of relevant values to bits ($b_{n-1}, b_{n-2}, \dots, b_1, b_0$) in the digital word are realized such as for the sampling capacitor (C_n).</p> <p>2. Method for conversion as claimed in claim 1 characterized in that after termination of accumulation of electric charge in the additional sampling capacitor (C_{nA}) and after detection of the beginning of the subsequent time interval (T_{x+2}) by means of the control module (CM), the next cycle begins and electric charge is delivered by the use of the current source and accumulated again in the sampling capacitor (C_n), or in the sampling capacitor (C_n) and in the capacitor (C_{n-1}) having the highest capacitance value in the array of redistribution which is connected</p>

to the sampling capacitor (C_n) in parallel.

3. Method for conversion as claimed in claim 1 and 2 **characterized in that** in a period of time when electric charge is delivered by the use of the current source and accumulated in the additional sampling capacitor (C_{nA}), a part of electric charge is accumulated simultaneously in the additional capacitor (C_{n-1A}) having the highest capacitance value in the array of redistribution which is connected to the additional sampling capacitor (C_{nA}) in parallel while a capacitance value of the additional capacitor (C_{n-1A}) having the highest capacitance value in the array of redistribution equals the capacitance value of the capacitor C_{n-1} having the highest capacitance value in the array of redistribution. 15
4. Method for conversion as claimed in claim 1, 2 and 3 **characterized in that** after termination of process of redistribution, the charge, accumulated in the last of capacitors on which the reference voltage (U_L) had not been reached when the process of redistribution was realized, is conserved. 20
5. Apparatus for clockless conversion of time interval to digital word comprising an array of redistribution whose control inputs are connected to control outputs of a control module and the control module is equipped with a digital output, a complete conversion output, a time interval signal input (InT), a first control input connected to an output of the first comparator and a second control input connected to an output of a second comparator whereas a source of auxiliary voltage, a section of a sampling capacitor and a second controlled current source are connected to the array of redistribution while a control input of the second controlled current source is connected to an output controlling the second current source and one end of the second current source is connected to a source rail and the other end of the second current source is connected to a destination rail and a voltage supply is connected to one end of the first current source whose control input is connected to an output controlling the first current source whereas the array of redistribution comprises sections whose number equals the number of bits in the digital word, and the section of the sampling capacitor and each section of the array of redistribution comprises a source on-off switch, a destination on-off switch, a ground change-over switch and at least one capacitor whose top plate is connected to the source rail through the source on-off switch and/or to the destination rail through the destination on-off switch and whose bottom plate is connected to ground of the circuit or to the source of auxiliary voltage through the ground change-over switch while a capacitance value of each capacitor of a given index in the array of redistribution is twice as high as a capacitance value of 25
6. Apparatus for conversion as claimed in claim 5 **characterized in that** at least one section in the array of redistribution (A) comprises the additional capacitor ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_0A$), the top plate change-over switches ($S_{Tn-1}, S_{Tn-2}, \dots, S_{T1}, S_{T0}; S_{Tn-1A}, S_{Tn-2A}, \dots, S_{T1A}, S_{T0A}$) and the bottom plate change-over switches ($S_{Bn-1}, S_{Bn-2}, \dots, S_{B1}, S_{B0}; S_{Bn-1A}, S_{Bn-2A}, \dots, S_{B1A}, S_{B0A}$) while the top plates of the capacitors ($C_{n-1}, C_{n-2}, \dots, C_1, C_0$) and the top plates of the additional capacitors ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_0A$) are connected appropriately to the source on-off switches ($S_{Hn-1}, S_{Hn-2}, \dots, S_{H1}, S_{H0}$) and to the destination on-off switches ($S_{Ln-1}, S_{Ln-2}, \dots, S_{L1}, S_{L0}$) or to the other end of the first current source (I) through the top plate change-over switches ($S_{Tn-1}, S_{Tn-2}, \dots, S_{TT}, S_{T0}; S_{Tn-1A}, S_{Tn-2A}, \dots, S_{T1A}, S_{T0A}$) whereas the bottom plates of the capacitors ($C_{n-1}, C_{n-2}, \dots, C_1, C_0$) and the bottom plates of the additional capacitors ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_0A$) are connected appropriately to the ground change-over switches ($S_{Gn-1}, S_{Gn-2}, \dots, S_{G1}, S_{G0}$) or to ground of 30 35 40 45 50 55

a capacitor of a previous index and also the destination rail is connected to ground of the circuit through the destination on-off switch and to a non-inverting input of the second comparator whose inverting input is connected to a source of the reference voltage and the source rail is connected to an inverting input of the first comparator whose non-inverting input is connected to the source of auxiliary voltage whereas control inputs of the source on-off switches and a control input of the destination rail on-off switch are connected appropriately to control outputs of the control module and control inputs of the destination on-off switches are coupled together and connected appropriately to the control outputs of the control module **characterized in that** the other end of the first current source (I) is connected to a section of the sampling capacitor (A_n) comprising an additional sampling capacitor (C_{nA}), top plate change-over switches (S_{Tn}, S_{TnA}), bottom plate change-over switches (S_{Bn}, S_{BnA}) while the top plate of the sampling capacitor (C_n) and the top plate of the additional sampling capacitor (C_{n-1}) are connected to the source on-off switch (S_{Hn}) and to the destination on-off switch (S_{Ln}) or to the other end of the first current source (I) through top plate change-over switches (S_{Tn}, S_{TnA}) whereas the bottom plate of the sampling capacitor (C_n) and the bottom plate of the additional sampling capacitor (C_{nA}) are connected to the ground change-over switches (S_{Gn}) or to ground of the circuit through the bottom plate change-over switches (S_{Bn}, S_{BnA}) and control inputs of the top plate change-over switches (S_{Tn}, S_{TnA}) and control inputs of the bottom plate change-over switches (S_{Bn}, S_{BnA}) are coupled together and connected appropriately to an output controlling the change-over switches of the plates (A_C).

6. Apparatus for conversion as claimed in claim 5 **characterized in that** at least one section in the array of redistribution (A) comprises the additional capacitor ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_0A$), the top plate change-over switches ($S_{Tn-1}, S_{Tn-2}, \dots, S_{T1}, S_{T0}; S_{Tn-1A}, S_{Tn-2A}, \dots, S_{T1A}, S_{T0A}$) and the bottom plate change-over switches ($S_{Bn-1}, S_{Bn-2}, \dots, S_{B1}, S_{B0}; S_{Bn-1A}, S_{Bn-2A}, \dots, S_{B1A}, S_{B0A}$) while the top plates of the capacitors ($C_{n-1}, C_{n-2}, \dots, C_1, C_0$) and the top plates of the additional capacitors ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_0A$) are connected appropriately to the source on-off switches ($S_{Hn-1}, S_{Hn-2}, \dots, S_{H1}, S_{H0}$) and to the destination on-off switches ($S_{Ln-1}, S_{Ln-2}, \dots, S_{L1}, S_{L0}$) or to the other end of the first current source (I) through the top plate change-over switches ($S_{Tn-1}, S_{Tn-2}, \dots, S_{TT}, S_{T0}; S_{Tn-1A}, S_{Tn-2A}, \dots, S_{T1A}, S_{T0A}$) whereas the bottom plates of the capacitors ($C_{n-1}, C_{n-2}, \dots, C_1, C_0$) and the bottom plates of the additional capacitors ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_0A$) are connected appropriately to the ground change-over switches ($S_{Gn-1}, S_{Gn-2}, \dots, S_{G1}, S_{G0}$) or to ground of 30 35 40 45 50 55

the circuit through the bottom plate change-over switches (S_{Bn-1} , S_{Bn-2} , ..., S_{B1} , S_{B0} ; S_{Bn-1A} , S_{Bn-2A} , ..., S_{B1A} , S_{B0A}) whereas the control inputs of the top plate change-over switches (S_{Tn-1} , S_{Tn-2} , ..., S_{T1} , S_{T0} ; S_{Tn-1A} , S_{Tn-2A} , ..., S_{T1A} , S_{T0A}) and the control inputs of the bottom plate change-over switches (S_{Bn-1} , S_{Bn-2} , ..., S_{B1} , S_{B0} ; S_{Bn-1A} , S_{Bn-2A} , ..., S_{B1A} , S_{B0A}) are coupled together and connected to the output controlling the change-over switches of the plates (A_C). 5

7. Apparatus for conversion as claimed in claim 6 **characterized in that** the capacitance value of the sampling capacitor (C_n) and the capacitance value of the additional sampling capacitor (C_{nA}) are not lower than the capacitance value of the capacitor (C_{n-1}) having the highest capacitance value in the array of redistribution. 10

8. Apparatus for conversion as claimed in claim 6 **characterized in that** the capacitance value of the additional capacitor (C_{n-1A} , C_{n-2A} , ..., C_{1A} , C_0A) in the array of redistribution is equal appropriately to the capacitance value of the capacitor (C_{n-1} , C_{n-2} , ..., C_1 , C_0) in the array of redistribution. 15

Patentansprüche

1. Verfahren für taktgeberfreie Umwandlung eines Zeitintervalls in ein digitales Wort, bei dem der Anfang und das Ende des Zeitintervalls von einem Steuermodul des Zeitintervalls erfasst und das Zeitintervall mittels einer zu dem Zeitintervall proportionalen, elektrischen Ladung, die während dieses Zeitintervalls mittels einer Stromquelle zugeführt und in einem Abtastkondensator oder in einem Abtastkondensator und mit ihm parallel geschalteten Kondensator mit der höchsten Kapazität in der Umverteilungseinheit angesammelt wird, dargestellt wird, und bei dem dann in der Umverteilungseinheit der Prozess der Umverteilung der angesammelten elektrischen Ladung mittels eines Steuermoduls durch die Änderung des Zustands der Signale von den jeweiligen Steuerausgängen umgesetzt wird, wobei die Umverteilungseinheit einen Satz von Verbindern, Schaltern und Kondensatoren solcher Art enthält, dass die Kapazität eines jeden Kondensators mit dem folgenden Index doppelt so groß ist wie die Kapazität des unmittelbar vorstehenden Kondensators, und bei dem den Bits des digitalen Wortes mittels eines Steuermoduls entsprechende Werte zugeordnet werden, **gekennzeichnet dadurch, dass** nach Abschluss der Ansammlung der elektrischen Ladung im Abtastkondensator (C_n) oder im Abtastkondensator (C_{nA}) und dem parallel geschalteten Kondensator (C_{n-1}) mit der höchsten Kapazität in der Umverteilungseinheit, und nach dem Erfassen des Anfangs des 30

nächsten Zeitintervalls (T_{x+1}) mittels des Steuermoduls (CM) die elektrische Ladung mittels einer Stromquelle zugeführt und in dem zusätzlichen Abtastkondensator (C_{nA}) gesammelt wird, und dann der Prozess der Umverteilung der in dem zusätzlichen Abtastkondensator (C_{nA}) angesammelten elektrischen Ladung umgesetzt und den Bits (b_{n-1} , b_{n-2} , ..., b_1 , b_0) des digitalen Wortes mittels Steuermoduls (CM) entsprechende Werte zugeordnet werden, wobei die Ansammlung der elektrischen Ladung im zusätzlichen Abtastkondensator (C_{nA}), der Prozess der Umverteilung der im zusätzlichen Abtastkondensator (C_{nA}) gespeicherten elektrischen Ladung und die Zuordnung der entsprechenden Werte zu Bits (b_{n-1} , b_{n-2} , ..., b_1 , b_0) des digitalen Wortes so wie für den Abtastkondensator (C_n) umgesetzt wird. 5

2. Verfahren nach Anspruch 1, **gekennzeichnet dadurch, dass**, nach Abschluss der Ansammlung der elektrischen Ladung in dem zusätzlichen Abtastkondensator (C_{nA}) und Erfassung des Anfangs des nächsten Zeitintervalls (T_{x+2}) mithilfe des Steuermoduls (CM) der nächste Zyklus beginnt und die elektrische Ladung mittels der Stromquelle zugeführt und wieder im Abtastkondensator (C_n) oder im Abtastkondensator (C_{nA}) und dem mit ihm parallel geschalteten Kondensator (C_{n-1}) mit der höchsten Kapazität in der Umverteilungseinheit angesammelt wird. 10
3. Verfahren nach Anspruch 1 und 2, **gekennzeichnet dadurch, dass** wenn die elektrische Ladung mittels einer Stromquelle zugeführt und in dem zusätzlichen Abtastkondensator (C_{nA}) angesammelt wird, ein Teil der zugeführten elektrischen Ladung gleichzeitig in dem zusätzlichen Kondensator (C_{n-1A}) mit der höchsten Kapazität in der Umverteilungseinheit, der parallel zu dem zusätzlichen Abtastkondensator (C_{nA}) geschaltet wird, angesammelt wird, wobei die Kapazität des zusätzlichen Kondensators (C_{n-1A}) mit der höchsten Kapazität in der Umverteilungseinheit gleich der Kapazität des Kondensators (C_{n-1}) mit der höchsten Kapazität in der Umverteilungseinheit ist. 15
4. Verfahren nach Anspruch 1, 2 und 3, **gekennzeichnet dadurch, dass** nach Abschluss des Prozesses der Umverteilung im letzten der Kondensatoren, in dem während des Prozesses der Umverteilung keine Referenzspannung (U_L) erreicht wurde, die angesammelte elektrische Ladung angesammelt bleibt. 20
5. Vorrichtung für taktgeberfreien Umwandlung eines Zeitintervalls in ein digitales Wort mit Umverteilungseinheit, deren Steuereingänge mit den Steuerausgängen des Steuermoduls verbunden sind, und das Steuermodul mit dem Ausgang des digitalen Wortes, 25

dem Ausgang des Umwandlungsabschlusses, dem Eingang des Zeitintervalls und dem ersten Steuereingang, der mit dem Ausgang des ersten Komparators verbunden ist, und dem zweiten Steuereingang, der mit dem Ausgang des zweiten Komparators verbunden ist, ausgestattet sind, und die Umverteileinheit mit der Hilfsspannungsquelle, dem Abtastkondensatorabschnitt und der zweiten gesteuerten Stromquelle verbunden ist, deren Steuereingang mit dem Steuerausgang über die zweite Stromquelle verbunden ist, wobei der erste Pol der zweiten Stromquelle mit dem Quellbus und der zweite Pol der zweiten Stromquelle mit dem Zielbus verbunden ist, und die Versorgungsspannungsquelle mit dem ersten Pol der ersten Stromquelle verbunden ist, deren Steuereingang mit dem Steuerausgang der ersten Stromquelle verbunden ist, wobei die Umverteileinheit Abschnitte enthält, deren Anzahl der Anzahl der Bits des digitalen Wortes entspricht, und der Abtastkondensatorabschnitt und jeder Abschnitt der Umverteileinheit einen Quellverbinder, einen Zielverbinder, einen Erdungsschalter und mindestens einen Kondensator, dessen obere Abdeckung mit dem Quellbus über den Quellverbinder und/oder mit dem Zielbus über den Zielverbinder verbunden ist, und die untere Abdeckung über den Erdungsschalter mit der Masse der Einheit oder mit der Hilfsspannungsquelle verbunden ist, enthalten, wobei in der Umverteileinheit die Kapazität eines jeden Kondensators mit dem folgenden Index doppelt so groß ist wie die Kapazität des unmittelbar vorstehenden Kondensators, und dazu der Zielbus mit der Einheitsmasse über den Zielbus-Verbinder und mit dem nichtintervierenden Eingang des zweiten Komparators verbunden ist, dessen intervierender Eingang mit der Referenzspannungsquelle verbunden ist, und der Quellbus mit dem intervierenden Eingang des ersten Komparators verbunden ist, dessen nichtintervierender Eingang mit einer Hilfsspannungsquelle verbunden ist, während die Steuereingänge der Quellverbinder und des Zielbus-Verbinder entsprechend mit den Steuerausgängen des Steuermoduls, und die Steuereingänge der Zielverbinder miteinander gekoppelt und mit den Steuerausgängen des Steuermoduls entsprechend verbunden sind, **gekennzeichnet dadurch, dass** der zweite Pol der ersten Stromquelle (I) mit dem Abtastkondensatorabschnitt (A_n), der einen zusätzlichen Abtastkondensator (C_{nA}) und Schalter der oberen Abdeckungen (S_{Tn}, S_{TnA}) und Schalter der unteren Abdeckungen (S_{Bn}, S_{BnA}) enthält, verbunden ist, wobei die oberen Abdeckungen des Abtastkondensators (C_n) und des zusätzlichen Abtastkondensators (C_{n-1}) über die Schalter der oberen Abdeckungen (S_{Tn}, S_{TnA}) mit dem Quellverbinder (S_{Hn}) und dem Zielverbinder (S_{Ln}) oder mit dem zweiten Pol der ersten Stromquelle (I) verbunden werden, wobei die unteren Abdeckungen des Abtastkondensators

(C_n) und des zusätzlichen Abtastkondensators (C_{nA}) über die Schalter der unteren Abdeckungen (S_{Bn}, S_{BnA}) mit dem Erdungsschalter (S_{Gn}) oder mit der Einheitsmasse verbunden werden, während die Steuereingänge der Schalter der oberen Abdeckungen (S_{Tn}, S_{TnA}) und der Schalter der unteren Abdeckungen (S_{Bn}, S_{BnA}) miteinander gekoppelt und mit dem Steuerausgang über die Schalter der Abdeckungen (A_c) entsprechend verbunden sind.

6. Vorrichtung nach Anspruch 5, **gekennzeichnet dadurch, dass** mindestens ein Abschnitt der Umverteileinheit (A) einen zusätzlichen Kondensator ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_{0A}$) und Schalter der oberen Abdeckungen ($S_{Tn-1}, S_{Tn-2}, \dots, S_{T1}, S_{T0}; S_{Tn-1A}, S_{Tn-2A}, \dots, S_{T1A}, S_{T0A}$) und Schalter der unteren Abdeckungen ($S_{Bn-1}, S_{Bn-2}, \dots, S_{B1}, S_{B0}; S_{Bn-1A}, S_{Bn-2A}, \dots, S_{B1A}, S_{B0A}$) enthält, wobei die oberen Abdeckungen der Kondensatoren ($C_{n-1}, C_{n-2}, \dots, C_1, C_0$) und der zusätzlichen Kondensatoren ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_{0A}$) entsprechend über die Schalter der oberen Abdeckungen ($S_{Tn-1}, S_{Tn-2}, \dots, S_{T1}, S_{T0}; S_{Tn-1A}, S_{Tn-2A}, \dots, S_{T1A}, S_{T0A}$) mit den Quellverbinder ($S_{Hn-1}, S_{Hn-2}, \dots, S_{H1}, S_{H0}$) und den Zielverbinder ($S_{Ln-1}, S_{Ln-2}, \dots, S_{L1}, S_{L0}$) oder mit dem zweiten Pol der ersten Stromquelle (I) verbunden werden, und die unteren Abdeckungen der Kondensatoren ($C_{n-1}, C_{n-2}, \dots, C_1, C_0$) und der zusätzlichen Kondensatoren ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_{0A}$) entsprechend über die Schalter der unteren Abdeckungen ($S_{Bn-1}, S_{Bn-2}, \dots, S_{B1}, S_{B0}; S_{Bn-1A}, S_{Bn-2A}, \dots, S_{B1A}, S_{B0A}$) mit Erdungsschaltern ($S_{Gn-1}, S_{Gn-2}, \dots, S_{G1}, S_{G0}$) oder mit der Einheitsmasse verbunden werden, wobei die Steuereingänge der Schalter der oberen Abdeckungen ($S_{Tn-1}, S_{Tn-2}, \dots, S_{T1}, S_{T0}; S_{Tn-1A}, S_{Tn-2A}, \dots, S_{T1A}, S_{T0A}$) und der Schalter der unteren Abdeckungen ($S_{Bn-1}, S_{Bn-2}, \dots, S_{B1}, S_{B0}; S_{Bn-1A}, S_{Bn-2A}, \dots, S_{B1A}, S_{B0A}$) miteinander gekoppelt und mit dem Steuerausgang über die Schalter der Abdeckungen (A_C) verbunden sind.
7. Vorrichtung nach Anspruch 6 **gekennzeichnet dadurch, dass** die Kapazitäten des Abtastkondensators (C_n) und des zusätzlichen Abtastkondensators (C_{nA}) nicht kleiner sind als die Kapazitäten des Kondensators (C_{n-1}) mit der höchsten Kapazität in der Umverteileinheit.
8. Vorrichtung nach Anspruch 6 **gekennzeichnet dadurch, dass** der zusätzliche Kondensator ($C_{n-1A}, C_{n-2A}, \dots, C_{1A}, C_{0A}$) der Umverteileinheit eine Kapazität aufweist, die der Kapazität des Kondensators ($C_{n-1}, C_{n-2}, \dots, C_1, C_0$) der Umverteileinheit entspricht.

Revendications

1. Procédé de conversion sans horloge d'un intervalle de temps en mot numérique, consistant à détecter à l'aide d'un module de commande le début et la fin d'un intervalle de temps et à reproduire cet intervalle de temps par une charge électrique proportionnelle, fournie pendant cet intervalle de temps au moyen d'une source de courant et accumulée dans un condensateur d'échantillonnage, ou dans un condensateur d'échantillonnage et un condensateur ayant la plus grande capacité et qui lui est connecté en parallèle dans une unité de redistribution, puis à réaliser dans l'unité de redistribution le processus de redistribution de la charge électrique accumulée, au moyen d'un module de commande en modifiant les états des signaux à partir des sorties de commande respectives, où l'unité de redistribution comprend un ensemble de connecteurs, de commutateurs et de condensateurs, de sorte que la capacité de chaque condensateur d'indice suivant soit deux fois plus grande que la capacité du condensateur qui le précède immédiatement et à attribuer au moyen d'un module de commande, des valeurs correspondantes des bits du mot numérique, **caractérisé en ce que**, après l'accumulation de la charge électrique dans le condensateur d'échantillonnage (C_n) ou dans le condensateur d'échantillonnage (C_n), et le condensateur (C_{n-1}) qui lui est connecté en parallèle et ayant la plus grande capacité dans l'unité de redistribution et la détection par le module de contrôle (CM) du début du prochain intervalle de temps (T_{x+1}), la charge électrique est fournie par une source de courant et s'accumule dans un condensateur d'échantillonnage supplémentaire (C_{nA}), puis s'effectue le processus de redistribution de la charge électrique accumulée dans le condensateur d'échantillonnage supplémentaire (C_{nA}) et les valeurs correspondantes des bits ($b_{n-1}, b_{n-2}, \dots, b_1, b_0$) du mot numérique sont affectées à l'aide du module de commande (CM), où l'accumulation de charge électrique dans le condensateur d'échantillonnage supplémentaire (C_{nA}), le processus de redistribution de la charge électrique accumulée dans le condensateur d'échantillonnage supplémentaire (C_{nA}) et l'attribution des valeurs des bits appropriées ($b_{n-1}, b_{n-2}, \dots, b_1, b_0$) du mot numérique sont effectués comme pour le condensateur d'échantillonnage (C_n). 5
2. Procédé selon la revendication 1, **caractérisé en ce que** après l'accumulation de la charge électrique dans le condensateur d'échantillonnage supplémentaire (C_{nA}) et la détection à l'aide du module de commande (CM) du début de l'intervalle de temps suivant (T_{x+2}), le cycle suivant commence et la charge électrique est fournie au moyen d'une source courant et s'accumule à nouveau dans le condensateur 10
- d'échantillonnage (C_n) ou dans le condensateur d'échantillonnage (C_n) et le condensateur qui lui est connecté en parallèle (C_{n-1}) ayant la plus grande capacité dans l'unité de redistribution. 15
3. Procédé selon les revendications 1 et 2, **caractérisé en ce que**, lorsque la charge électrique est fournie à l'aide d'une source de courant et s'accumule dans un condensateur d'échantillonnage supplémentaire (C_{nA}), en même temps une partie de la charge électrique fournie s'accumule dans le condensateur supplémentaire (C_{n-1A}) ayant la plus grande capacité dans l'unité de redistribution, connecté en parallèle à un condensateur d'échantillonnage supplémentaire (C_{nA}), où la capacité du condensateur supplémentaire (C_{n-1A}) ayant la plus grande capacité dans l'unité de redistribution est égale à la capacité du condensateur (C_{n-1}) ayant la plus grande capacité dans l'unité de redistribution. 20
4. Procédé selon les revendications 1, 2 et 3, **caractérisé en ce que** après la fin du processus de redistribution, dans le dernier des condensateurs, sur lequel la tension de référence (U_L) n'a pas été obtenue pendant le processus de redistribution, la charge électrique accumulée y est laissée. 25
5. Appareil de conversion sans horloge d'un intervalle de temps en mot numérique, contenant une unité de redistribution, dont les entrées de commande sont connectées aux sorties de commande du module de commande, et le module de commande est équipé d'une sortie de mot numérique, d'une sortie de fin de traitement, d'une entrée d'intervalle de temps ainsi que d'une première entrée de commande, connectée à la sortie du premier comparateur et la deuxième entrée de commande connectée à la sortie du deuxième comparateur, par contre à l'unité de redistribution sont connectées la source de tension auxiliaire, la section de condensateur d'échantillonnage et la deuxième source de courant commandée, dont l'entrée de commande est reliée à la sortie de commande de la deuxième source de courant, où le premier pôle de la deuxième source de courant est connecté au rail source, et le deuxième pôle de la deuxième source de courant est connecté au rail cible, et la source de la tension d'alimentation est connectée au premier pôle de la première source de courant, dont l'entrée de commande est connectée à la sortie de commande de la première source de courant, où l'unité de redistribution comprend des sections dont le nombre est égal au nombre de bits du mot numérique, et la section de condensateur d'échantillonnage et chaque section d'unité de redistribution comprend un connecteur source, un connecteur cible, un commutateur de masse et au moins un condensateur dont le couvercle supérieur est connecté au rail source, via 30
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le connecteur source, et/ou au rail cible via le connecteur cible, et le couvercle inférieur via l'interrupteur de masse, est connecté à la masse du système ou à la source de tension auxiliaire, où dans l'unité de redistribution, la capacité de chaque condensateur d'indice suivant est deux fois plus grande que la capacité du condensateur qui le précède immédiatement ; de plus, le rail cible est connecté à la masse du système via le connecteur de rail cible et à l'entrée non inverseuse du deuxième comparateur, dont l'entrée inverseuse est connectée à la source de tension de référence, et le rail source est connecté à l'entrée inverseuse du premier comparateur, dont l'entrée non inverseuse est connectée à la source de tension auxiliaire, tandis que les entrées de commande des connecteurs sources ainsi que du connecteur de rail cible sont connectées, respectivement, aux sorties de commande du module de commande et les entrées de commande des connecteurs cibles sont couplées l'une à l'autre et connectées, respectivement, aux sorties de commande du module de commande, **caractérisé en ce que le deuxième pôle de la première source de courant (I)** est connecté à la section du condensateur d'échantillonnage (A_n), qui comprend le condensateur d'échantillonnage supplémentaire (C_{nA}) ainsi que les commutateurs des couvercles supérieurs (S_{Tn} , S_{TnA}) et les commutateurs des couvercles inférieurs (S_{Bn} , S_{BnA}), où les couvercles supérieurs du condensateur d'échantillonnage (C_n) et du condensateur d'échantillonnage supplémentaire (C_{n-1}) sont connectés via les commutateurs des couvercles supérieurs (S_{Tn} , S_{TnA}) avec le connecteur source (S_{Hn}) et le connecteur cible (S_{Ln}) ou avec le deuxième pôle de la première source de courant (I), tandis que les couvercles inférieurs du condensateur d'échantillonnage (C_n) et du condensateur d'échantillonnage supplémentaire (C_{nA}) sont connectés via les commutateurs des couvercles inférieurs (S_{Bn} , S_{BnA}) avec le commutateur de masse (S_{Gn}) ou avec la masse de l'unité, et les entrées de commande des commutateurs des couvercles supérieurs (S_{Tn} , S_{TnA}) ainsi que des commutateurs des couvercles inférieurs (S_{Bn} , S_{BnA}) sont couplés l'un à l'autre et connectés à la sortie respectivement avec la sortie de commande des commutateurs des couvercles (A_C). 50

6. Appareil selon la revendication 5, **caractérisé en ce qu'au moins une section de l'unité de redistribution (A) comprend un condensateur supplémentaire (C_{n-1A} , C_{n-2A} , ..., C_{1A} , C_{0A}) ainsi que les commutateurs des couvercles supérieurs (S_{Tn-1} , S_{Tn-2} , ..., S_{T1} , S_{T0} , S_{Tn-1A} , S_{Tn-2A} , ..., S_{T1A} , S_{T0A}) et les commutateurs des couvercles inférieurs (S_{Bn-1} , S_{Bn-2} , ..., S_{B1} , S_{B0} , S_{Bn-1A} , S_{Bn-2A} , ..., S_{B1A} , S_{B0A}), où les cou-**

vercles supérieurs des condensateurs (C_{n-1} , C_{n-2} , ..., C_1 , C_0) et des condensateurs supplémentaires (C_{n-1A} , C_{n-2A} , ..., C_{1A} , C_{0A}) sont connectés, respectivement, via les commutateurs des couvercles supérieurs (S_{Tn-1} , S_{Tn-2} , ..., S_{T1} , S_{T0} , S_{Tn-1A} , S_{Tn-2A} , ..., S_{T1A} , S_{T0A}) avec les connecteurs sources (S_{Hn-1} , S_{Hn-2} , ..., S_{H1} , S_{H0}) et les connecteurs cibles (S_{Ln-1} , S_{Ln-2} , ..., S_{L1} , S_{L0}) ou avec le second pôle de la première source de courant (I), tandis que les couvercles inférieurs des condensateurs (C_{n-1} , C_{n-2} , ..., C_1 , C_0) et des condensateurs supplémentaires (C_{n-1A} , C_{n-2A} , ..., C_{1A} , C_{0A}) sont raccordés, respectivement, via les commutateurs des couvercles inférieurs (S_{Bn-1} , S_{Bn-2} , ..., S_{B1} , S_{B0} , S_{Bn-1A} , S_{Bn-2A} , ..., S_{B1A} , S_{B0A}) avec les commutateurs de masse (S_{Gn-1} , S_{Gn-2} , ..., S_{G1} , S_{G0}) ou avec la masse du système, et les entrées de commande des commutateurs des couvercles supérieurs (S_{Tn-1} , S_{Tn-2} , ..., S_{T1} , S_{T0} , S_{Tn-1A} , S_{Tn-2A} , ..., S_{T1A} , S_{T0A}) et les commutateurs des couvercles inférieurs (S_{Bn-1} , S_{Bn-2} , ..., S_{B1} , S_{B0} , S_{Bn-1A} , S_{Bn-2A} , ..., S_{B1A} , S_{B0A}) sont couplés l'un à l'autre et sont connectés à la sortie de commande des commutateurs des couvercles (A_C). 20

- 25 7. Appareil selon la revendication 6, **caractérisé en ce que** les capacités du condensateur d'échantillonnage (C_n) et du condensateur d'échantillonnage supplémentaire (C_{nA}) ne sont pas inférieures à la capacité du condensateur (C_{n-1}) qui a la plus grande capacité dans l'unité de redistribution. 30
8. Appareil selon la revendication 6, **caractérisé en ce que** le condensateur supplémentaire (C_{n-1A} , C_{n-2A} , ..., C_{1A} , C_{0A}) de l'unité de redistribution a une capacité égale, respectivement, à la capacité du condensateur (C_{n-1} , C_{n-2} , ..., C_1 , C_0) de l'unité de redistribution. 35

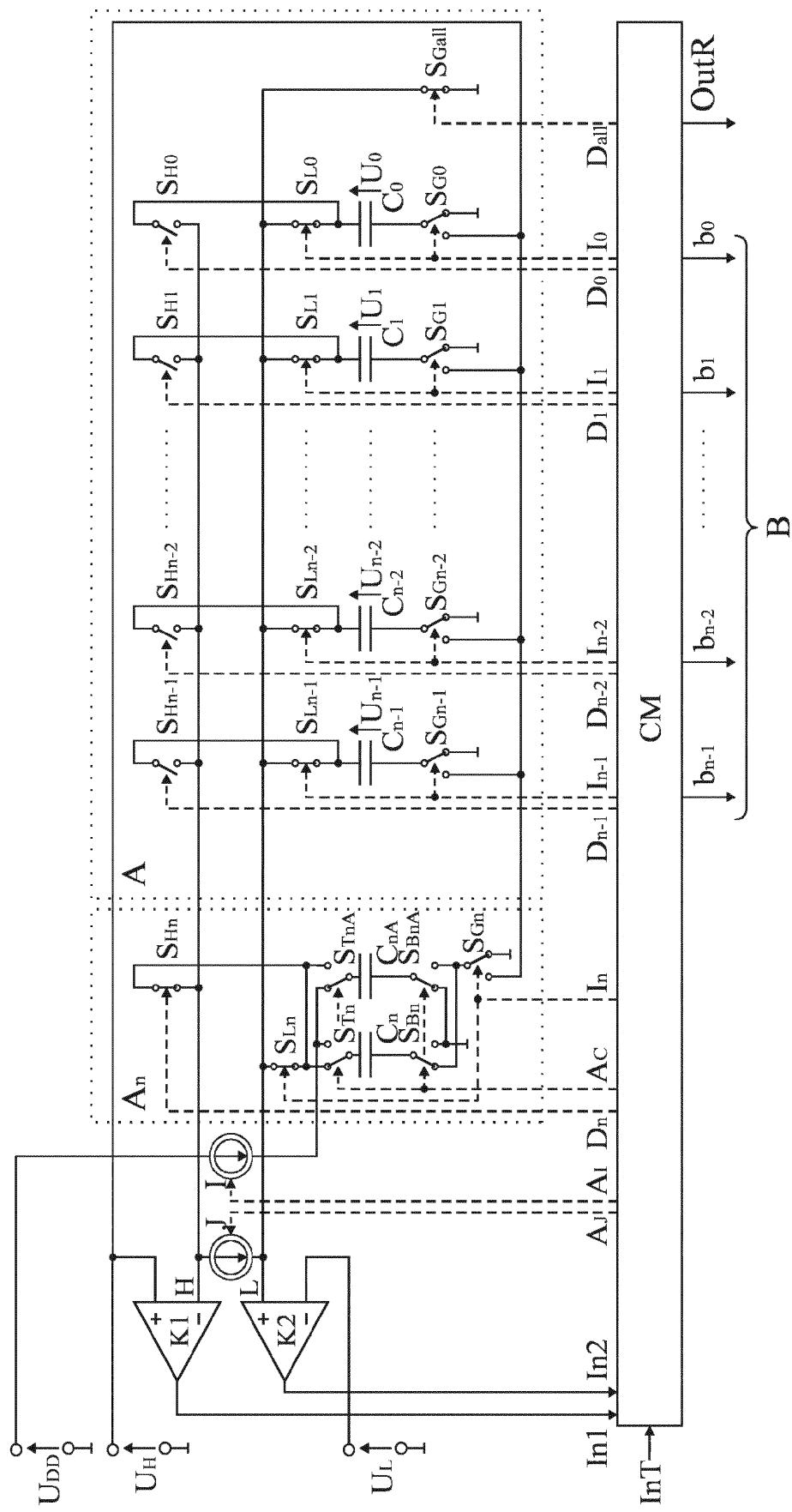
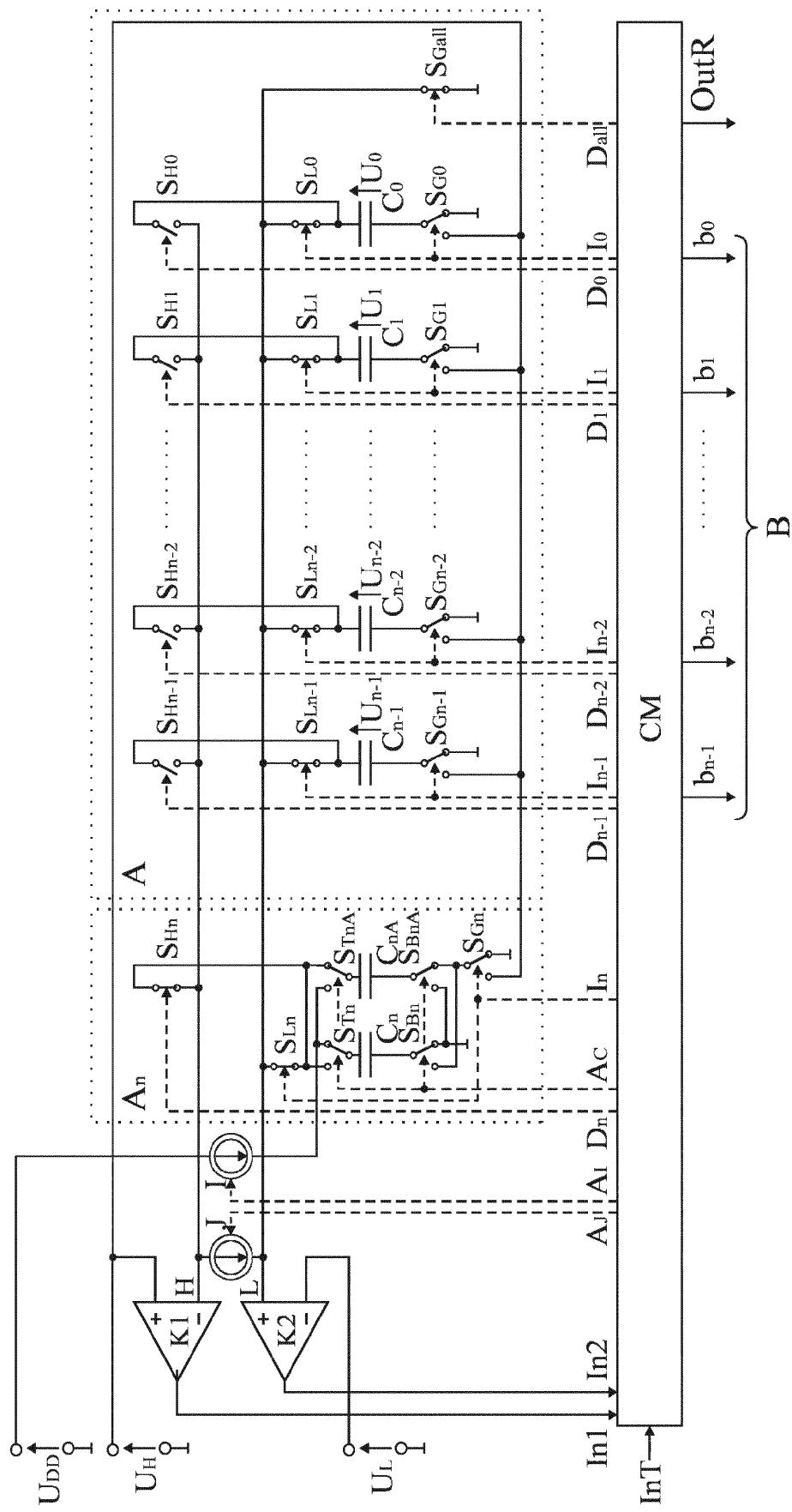


Fig. 1



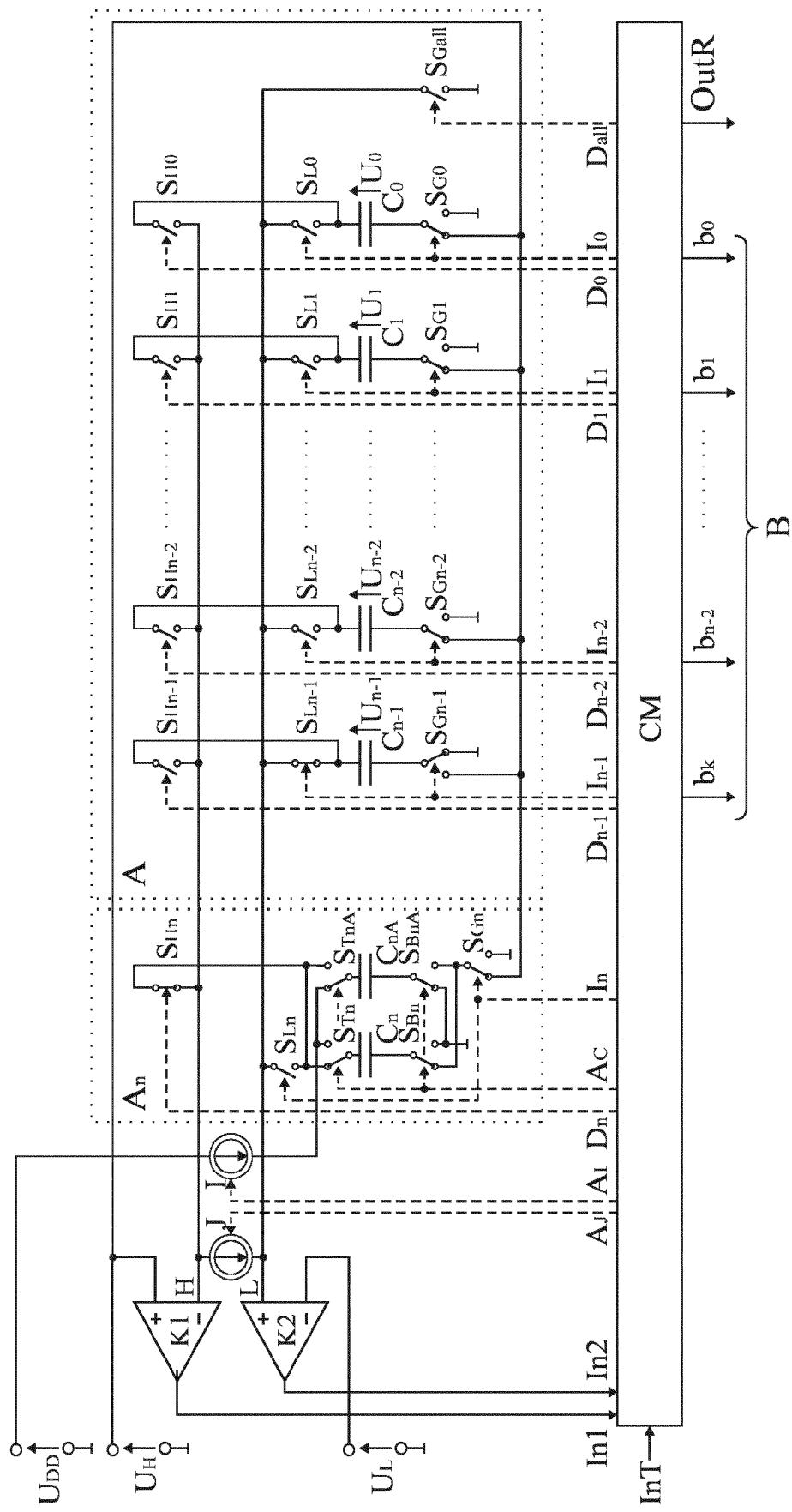


Fig. 3

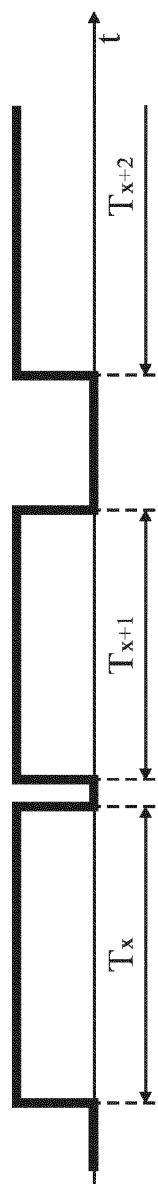


Fig. 4

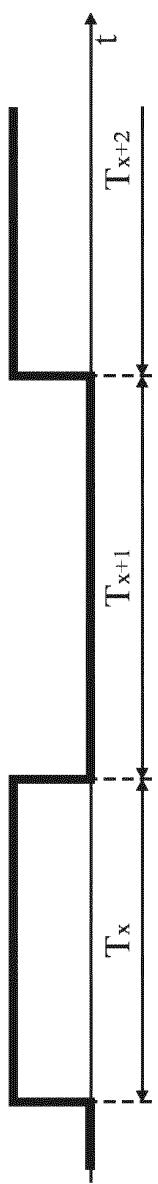


Fig. 5

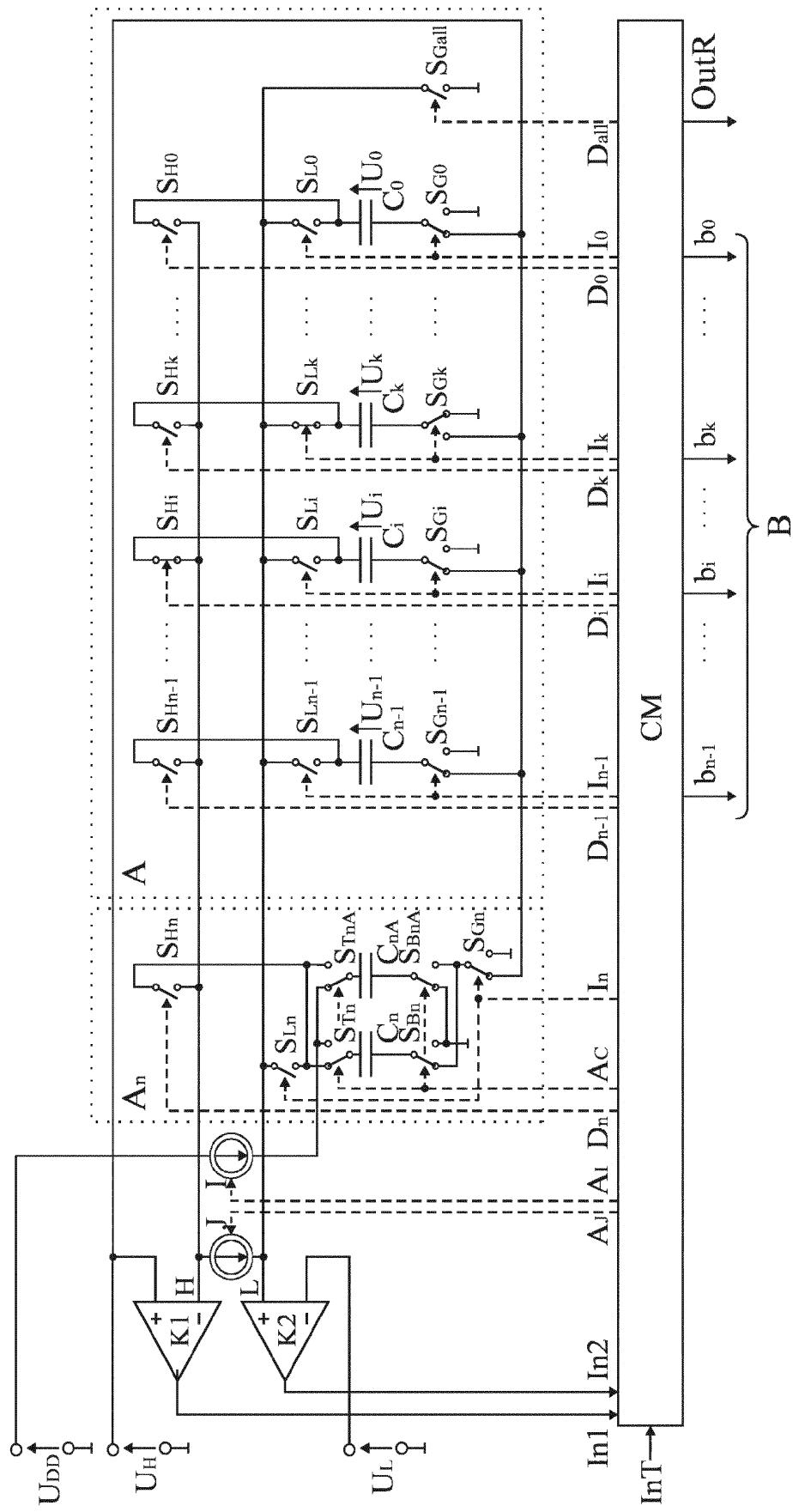


Fig. 6

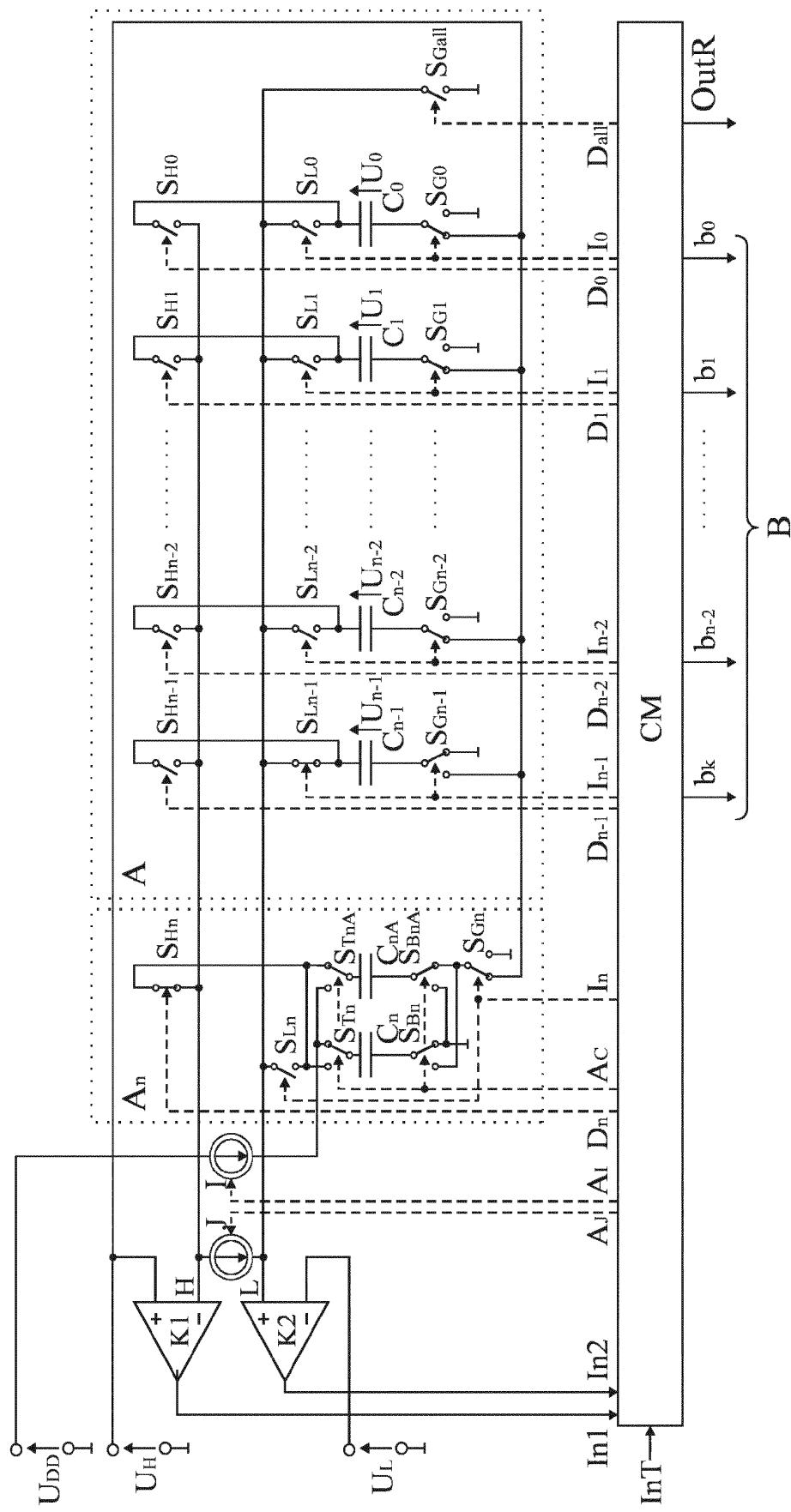


Fig. 7

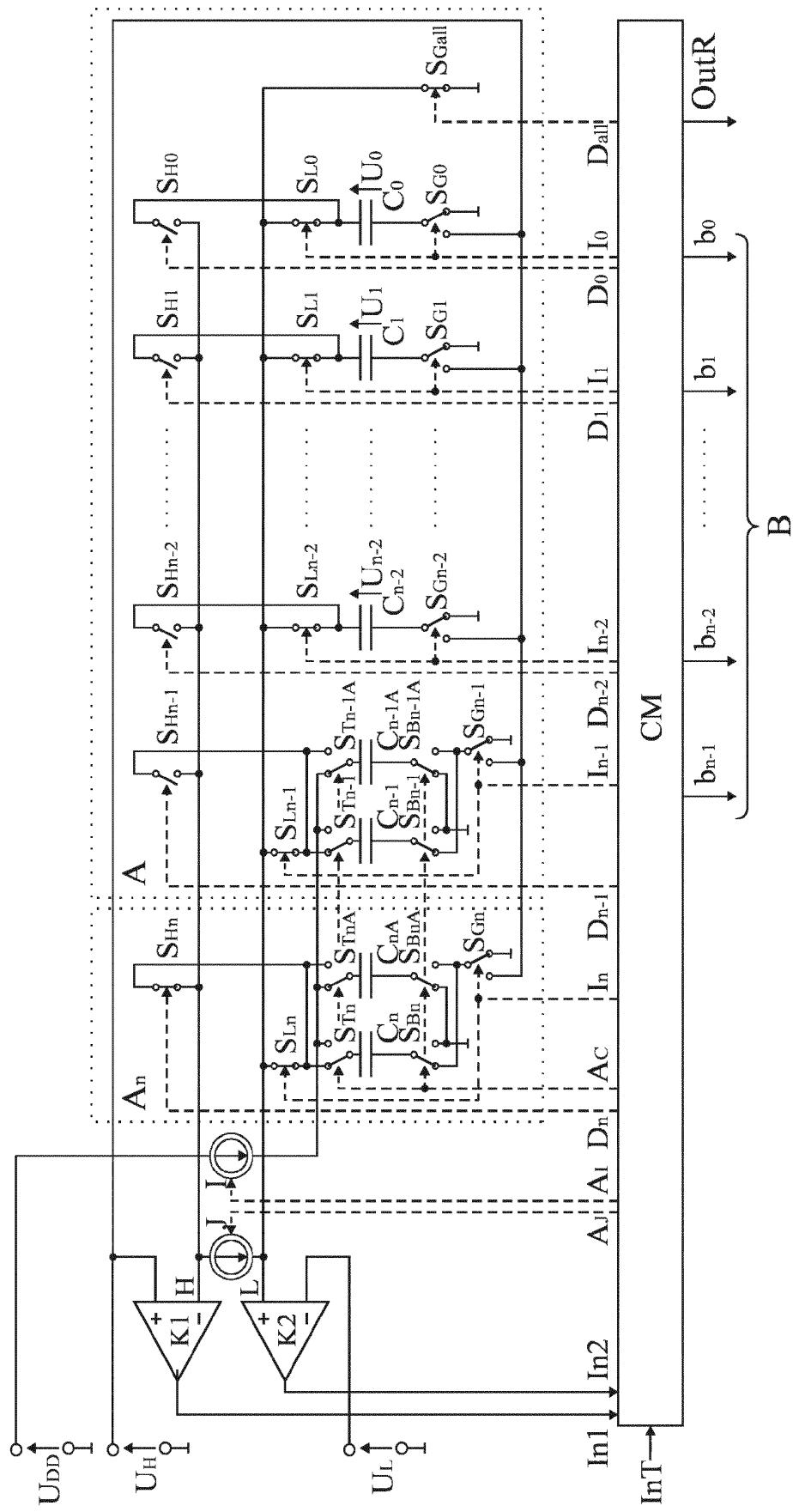


Fig. 8

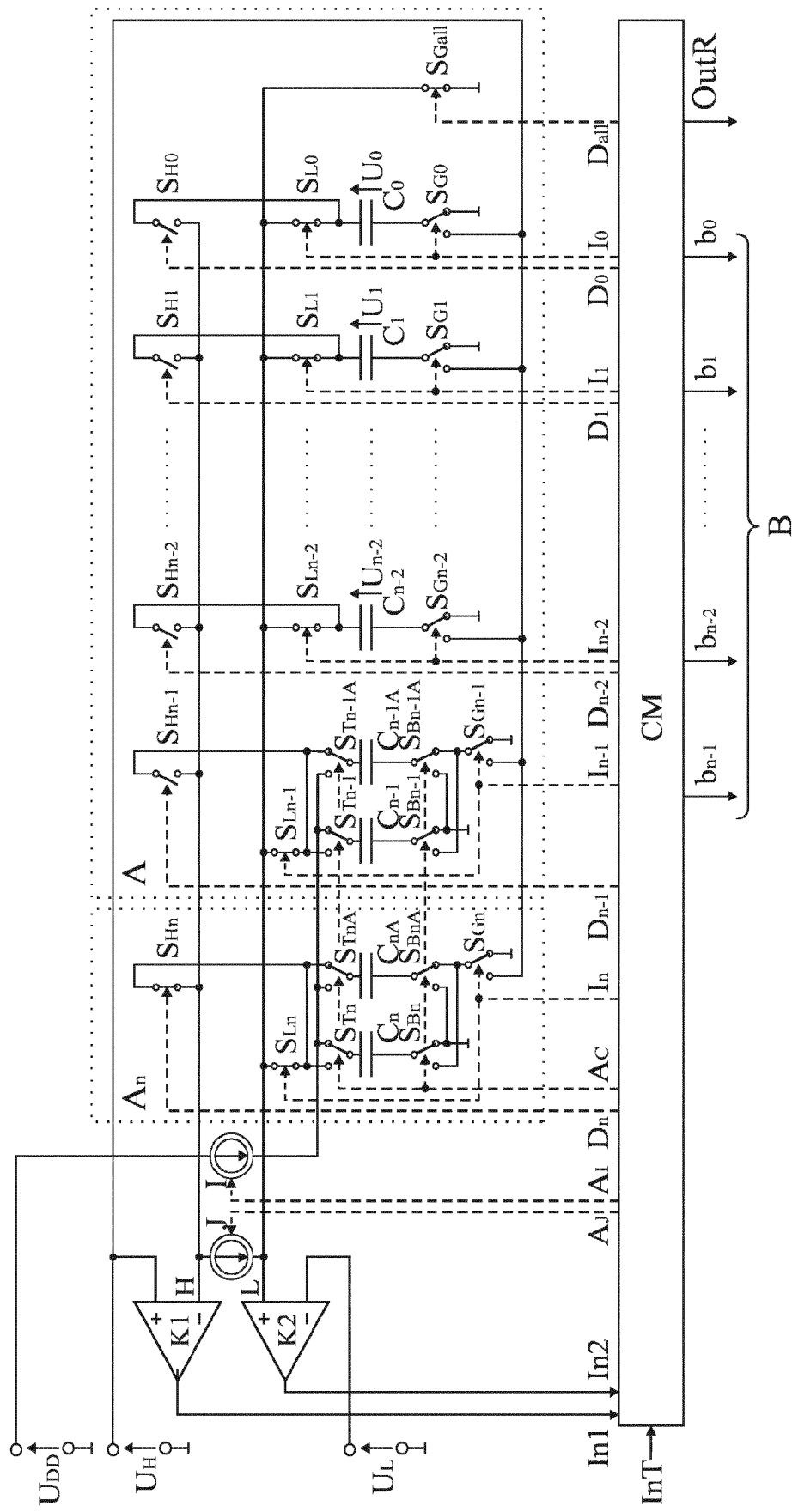


Fig. 9

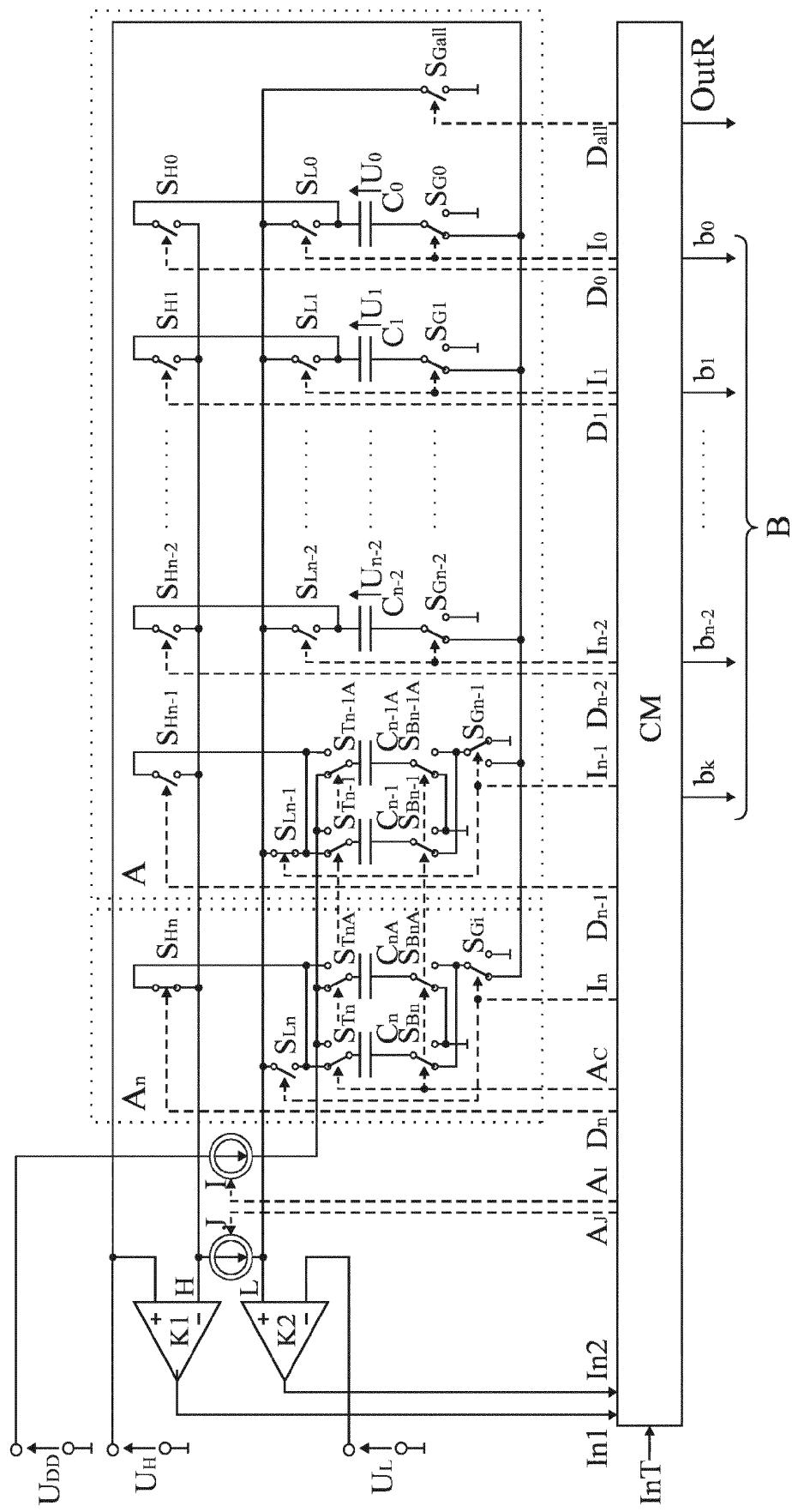


Fig. 10

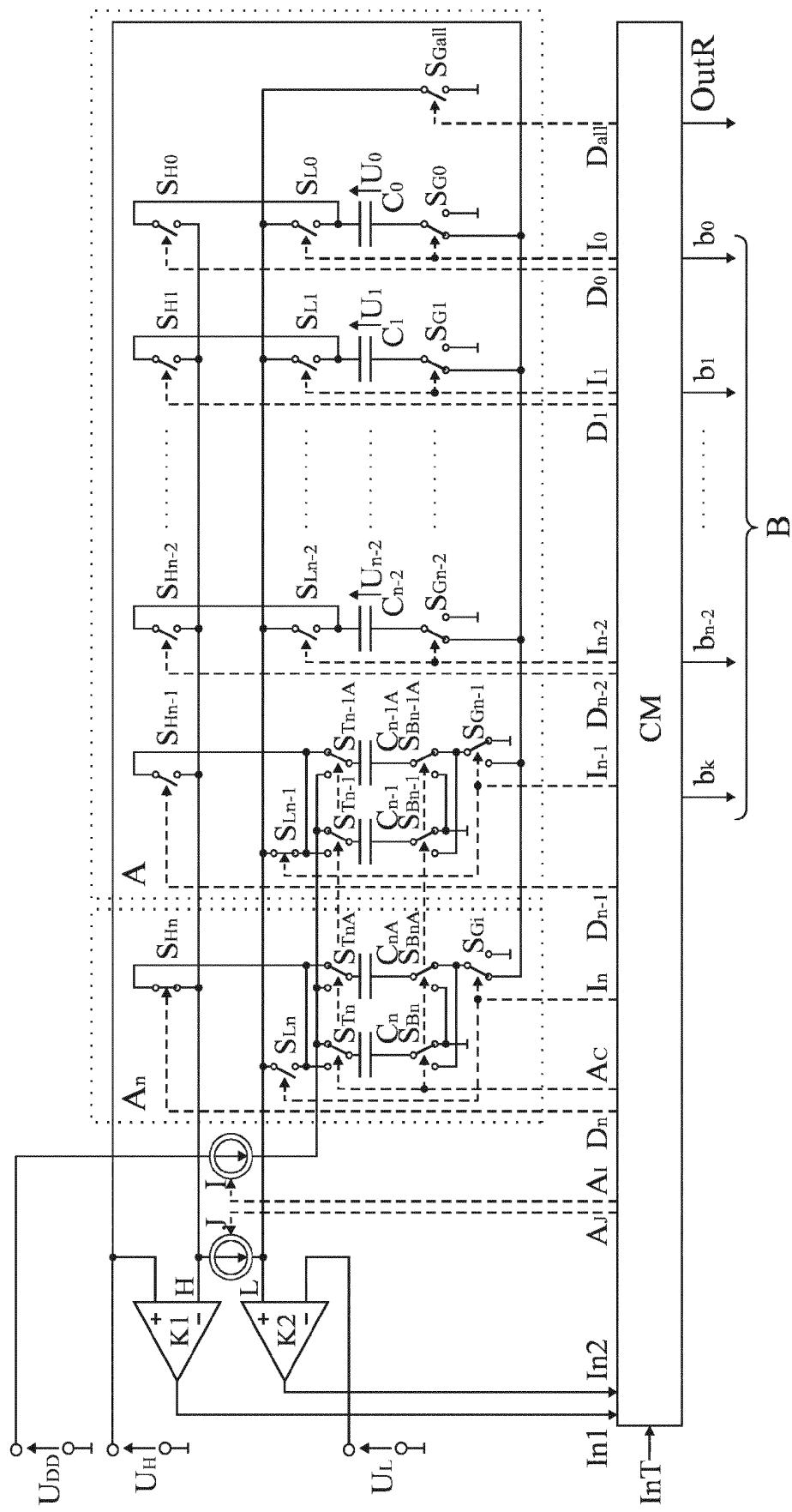


Fig. 11

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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