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(54) METHOD AND APPARATUS FOR CONVERSION OF VOLTAGE VALUE TO DIGITAL WORD

VERFAHREN UND VORRICHTUNG ZUR UMWANDLUNG EINES SPANNUNGSWERTES IN EIN DIGITALES WORT

PROCÉDÉ ET APPAREIL POUR CONVERSION DE VALEUR DE TENSION EN MOT NUMÉRIQUE

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Description

[0001] The subject of this invention is a method and an apparatus for conversion of an voltage value to a digital word that can be applied in monitoring and control systems.

[0002] The method for performing analog to digital conversion in a conversion circuit according to the document US 7164379 comprises a first stage configurable in an integration mode for integrating an analog signal and configurable in a folding mode for folding an integrated analog signal to generate a residue responsive to the analog signal, while the method comprises connecting the integrate and fold circuit to an analog signal source providing an analog signal to be converted during an integration mode; and disconnecting the integrate and fold circuit from the analog source during a folding mode.

[0003] The method for analog to digital conversion according to the document US 2006/0038712 using a multichannel analog to digital conversion circuit and wherein the multichannel analog to digital conversion circuit includes a plurality of linearized channels wherein each channel comprises a multi-stage pipelined charge-to-digital converter and an integrating capacitor within each stage of the four-stage converter, the integrating capacitor storing a charge proportional to an integral of an input charge.

[0004] The method for the conversion of the voltage signal to the digital signal known from the article (James McCreary, Paul R. Gray ,,A High-Speed, All-MOS Successive-Approximation Weighted Capacitor A/D Conversion Technique", Proceedings of IEEE International Solid-State Circuits Conference, February 1975, pp. 38-39) exploits the electric charge redistribution in the array of capacitors according to the successive approximation algorithm. The first stage of this method is sampling an instantaneous value of the input voltage signal consisting in accumulation of electric charge whose value is directly proportional to the input voltage value in the array of capacitors connected in parallel. The capacitance value of each given capacitor is twice as high as the capacitance value of the previous capacitor in the array, and one of plates of each capacitor is connected to the first common rail. As soon as sampling is terminated, the process of conversion of the accumulated charge value to a digital word is realized through its appropriate redistribution among the capacitors in the array. The conversion process is started from moving the other plate of the capacitor having the highest capacitance value to the reference potential of a desired value. A state of the switches exploited for this purpose is controlled by a synchronous sequential control module that generates relevant control signals. The charge redistribution among the capacitors in the array, which is enforced in this way, causes a change of a resultant potential of the first common rail. This potential is compared to the potential of the ground of the circuit by the use of a comparator. If the resultant potential of the first rail after changing the potential of the other plate of a given capacitor is higher than the potential of the ground of the circuit, this plate is moved back to the potential of the ground of the circuit, and the relevant bit in a digital word corresponding to this capacitor is set to zero. Otherwise, the other plate of this capacitor is left on the reference potential, and the relevant bit in a digital word is set to one. Afterwards, the potential of the other plate of the next capacitor of twice lower capacitance value is changed by means of the control module, and after that, the cycle is repeated until the whole digital word having a number of bits equal to n is generated where a duration of the sampling stage and a duration of successive steps of the conversion process is determined by period of the clock signal that clocks the circuit operation.

[0005] The time-to-digital converter according to the document US 2008/136698 includes two delay lines, comparators, and an encoder. Both delay line are connected serially and include resistors coupled in series. The comparators compare first voltages of nodes on the first delay line with second voltages of corresponding nodes on the second delay line. The encoder generates a digital code based on outputs of the comparators.

[0006] The apparatus for analog to digital conversion according to the document US 7164379 comprises a first circuit for receiving an analog signal applied to an input of the first circuit via a connection to an analog source and generating a first residue of the analog signal at an output, the first circuit selectively configurable in a first mode for integrating the analog signal to generate an integrated analog signal and configurable in a second mode for disconnecting the first circuit from the analog source while folding the integrated analog signal to generate the first residue; and a second circuit coupled to the output of the first circuit for resolving the first residue provided by the first circuit and for generating a further resolved second residue.

[0007] The apparatus for multi-channel analog to digital conversion according to the document US 2006/0038712 comprises a plurality of linearized channels wherein each channel comprises a multi-stage pipelined charge-to-digital converter and an integrating capacitor within each stage of the multi-stage converter, wherein analog residue is processed by subsequent analog to digital converter stages; and wherein each stage of respective linearized channels is configured for calculating gain and offset of each respective stage and wherein the gain and offset of a given stage is calculated using a result of a calculated gain and/or offset from an adjacent stage.

[0008] The voltage analog-to-digital converter known from the article (James McCreary, Paul R. Gray ,,A High-Speed, All-MOS Successive-Approximation Weighted Capacitor A/D Conversion Technique", Proceedings of IEEE International Solid-State Circuits Conference, February 1975, pp. 38-39) comprises the successive approximation capacitor array whose one input is connected to the source of converted input voltage, whereas the other input is connected to the

source of the reference voltage while its output is connected to the sequential control module through the comparator. The sequential control module is equipped with the digital output and the input of the clock signal that clocks a course of the conversion process. Two control outputs of the sequential control module are connected to the comparator, and the other control outputs are connected to the successive approximation capacitor array. The successive approximation capacitor array comprises a number of n capacitors of binary-weighted capacitance values and an additional capacitor while the first plate of each capacitor in the array is connected to the first common rail, and the capacitance value of the additional capacitor equals the capacitance value of the smallest capacitor in the array. The other plates of the capacitors in the array are connected to the other common rail through the change-over switches whose other stationary contacts are connected to the ground of the circuit. The first common rail is connected to the non-inverting input of the comparator, and the second common rail is connected through another switch to the source of the input voltage or to the source of the reference voltage while the inverting input of the comparator is connected to the ground of the circuit. The present invention is defined by the method according to claim 1 and the apparatus according to claim 3. Further embodiments are defined in the dependent claims. The method and the apparatus for conversion of a voltage value to a digital word according to the invention is characterized by simplicity of design. Furthermore, the use of the external gate signal and the comparators output signals for indication of instants of appropriate state transitions in the apparatus enables an external source of clock signal consuming considerable amount of energy to be eliminated, and thus, it causes a significant reduction of energy consumption by the apparatus.

The accumulation of charge in the sampling capacitor and at the same time in the capacitor having the highest capacitance value in the array of capacitors allows the required capacitance value of the sampling capacitor to be reduced twice with the same maximum value of voltage obtained on the sampling capacitor. Moreover, it also allows the duration of the transfer of charge accumulated in the sampling capacitor to subsequent capacitors in the array to be decreased.

Delivery of charge, which is accumulated in the sampling capacitor, or in the sampling capacitor and at the same time in the capacitor having the highest capacitance value in the array of capacitors, by the use of the current source allows the load of the source of the converted voltage to be constrained by the current source effectiveness.

The use of two current sources whose effectivenesses are well chosen allows the conversion time to be limited while the required conversion accuracy may be guaranteed at the same time.

[0009] The solution according to the invention is presented in the following figures:

Fig. 1 illustrates the block diagram of the apparatus.

Fig. 2 illustrates the schematic diagram of the apparatus in the relaxation phase.

Fig. 3 illustrates the schematic diagram of the apparatus at time of starting the conversion cycle: the charge accumulation in the sampling capacitor C_n connected in parallel to the source of the converted voltage U_{IN}.

Fig. 4 illustrates the schematic diagram of the apparatus during the charge transfer from the source capacitor C_i to the destination capacitor C_k for i=n and k=n-1.

Fig. 5 illustrates the schematic diagram of the apparatus during the transfer of charge from the source capacitor C_i to the destination capacitor C_k.

Fig. 6 illustrates the schematic diagram of the another version of the apparatus in the relaxation phase.

Fig. 7 illustrates the schematic diagram of the another version of the apparatus at time of starting the conversion cycle: charge accumulation both in the sampling capacitor C_n and in the capacitor C_{n-1} connected both in parallel to the source of the converted voltage U_{IN}.

Fig. 8 illustrates the block diagram of the another variant of the apparatus.

Fig. 9 illustrates the schematic diagram of the another variant of the apparatus in the relaxation phase.

Fig. 10 illustrates the schematic diagram of the another variant of the apparatus at time of starting the conversion cycle: accumulation of charge delivered by the use of the current source I in the sampling capacitor C_n.

Fig. 11 illustrates the schematic diagram of the another version of the apparatus during the transfer of charge from the source capacitor C_i to the destination capacitor C_k for i=n and k=n-1.

Fig. 12 illustrates the schematic diagram of the another version of the apparatus during the transfer of charge from the source capacitor C_i to the destination capacitor C_k.

Fig. 13 illustrates the schematic diagram of the another version of the other apparatus variant at time of starting the conversion cycle: accumulation of charge delivered by the use of the current source I both in the sampling capacitor C_n and in the capacitor C_{n-1} connected in parallel.

Fig. 14 illustrates the block diagram of the another variant of the apparatus.

Fig. 15 illustrates the schematic diagram of the another variant of the apparatus in the relaxation phase.

Fig. 16 illustrates the schematic diagram of the another variant of the apparatus at time of starting the conversion cycle: accumulation of charge delivered by the use of the current source I in the sampling capacitor C_n.

Fig. 17 illustrates the schematic diagram of the another version of the apparatus during the transfer of charge from the source capacitor C_i to the destination capacitor C_k for i=n and k=n-1.

Fig. 18 illustrates the schematic diagram of the another version of the apparatus during the transfer of charge from

the source capacitor C_i to the destination capacitor C_k.

Fig. 19 illustrates the schematic diagram of the another version of the other apparatus variant at time of starting the conversion cycle: accumulation of charge delivered by the use of the current source I both in the sampling capacitor C_n and in the capacitor C_{n-1} connected in parallel.

[0010] The method according to the invention consists in that after detecting the beginning of the active state of the signal on the trigger input InS by means of the control module CM, the converted voltage value is mapped to the portion of electric charge proportional to this converted voltage value, and the portion of charge is accumulated in the sampling capacitor C_n by connecting the sampling capacitor C_n in parallel to the source of the converted voltage U_{IN} during the active state of the signal on the trigger input InS, while the duration of the active state of the signal on the trigger input InS is not shorter than the assumed minimum value. After detecting the end of the active state of the signal on the trigger input InS by means of the control module CM, the function of the source capacitor C_i whose, index is defined by the content of the source capacitor C_i index register in the control module, CM is assigned by means of the control module CM to the sampling capacitor C_n by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register, and at the same time the function of the destination capacitor C_k, whose index is defined by the content of the destination capacitor C_k index register in the control module CM, is assigned by means of the control module CM to the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors while a capacitance value of each capacitor C_{n-1}, C_{n-2}, ..., C_1, C_0 of a given index is twice as high as a capacitance value of the capacitor of the previous index, by writing the value of the index of the capacitor C_{n-1} to the destination capacitor C_k index register. Afterwards, the process of redistribution of the accumulated charge in capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A is realized during which charge accumulated in the source capacitor C_i is transferred to the destination capacitor C_k by the use of the current source I, and at the same time the voltage U_k increasing on the destination capacitor C_k is compared to the reference voltage U_L value by the use of the second comparator K2, and also the voltage U_i on the source capacitor C_i is observed by the use of the first comparator K1. When the voltage U_i on the source capacitor C_i observed by the use of the first comparator K1 equals zero during the charge transfer, the function of the source capacitor C_i is assigned to the current destination capacitor C_k by means of the control module CM on the basis of the output signal of the first comparator K1 by writing the current content of the destination capacitor C_k index register in the control module CM to the source capacitor C_i index register in the control module CM, and also the function of the destination capacitor C_k is assigned to the subsequent capacitor in the array A whose capacitance value is twice lower than the capacitance value of the capacitor that operated as the destination capacitor directly before by reducing the content of the destination capacitor C_k index register by one, and charge transfer from a new source capacitor C_i to a new destination capacitor C_k is continued by the use of the current source I. When the voltage U_k on the destination capacitor C_k observed by the use of the second comparator K2 equals the reference voltage U_L value during the transfer of charge from the source capacitor C_i to the destination capacitor C_k, the function of the destination capacitor C_k is assigned by means of the control module CM on the basis of the output signal of the second comparator K2 to the subsequent capacitor in the array A whose capacitance value is twice lower than the capacitance value of the capacitor that operated as the destination capacitor directly before by reducing the content of the destination capacitor C_k index register by one, and also the charge transfer from the source capacitor C_i to a new destination capacitor C_k is continued. This process is still controlled by means of the control module CM on the basis of the output signals of the comparators K1 and K2 until the voltage U_i on the source capacitor C_i observed by the use of the first comparator K1 equals zero during the period in which the function of the destination capacitor C_k is assigned to the capacitor Co having the lowest capacitance value in the array A of capacitors, or the voltage Uo increasing on the capacitor Co and observed at the same time by the use of the second comparator K2 equals the reference voltage U_L value. The value one is assigned to these bits in the digital word, corresponding to the capacitors in the array A of capacitors, on which the voltage equal to the reference voltage U_L value has been obtained, and the value zero is assigned to the other bits by means of the control module CM.

[0011] In the another variant of the method, after detecting the beginning of the active state of the signal on the trigger input InS by means of the control module CM, electric charge is accumulated in the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors and at the same time in the sampling capacitor C_n connected in parallel to the capacitor C_{n-1} in the array A of capacitors where the capacitance value of the sampling capacitor C_n is not smaller than the capacitance value of the capacitor C_{n-1}, by connecting at the same time both capacitors (C_n) and (C_{n-1}) in parallel to the source of the converted voltage U_{IN} during the active state of the signal on the trigger input InS. After detecting the end of the active state of the signal on the trigger input InS by means of the control module CM, the function of the source capacitor C_i, whose index is defined by the content of the source capacitor C_i index register in the control module CM, is assigned by means of the control module CM to the sampling capacitor C_n by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register. At the same time, the function of the destination capacitor C_k, whose index is defined by the content of the destination capacitor C_k index register in the control module CM, is assigned by means of the control module CM to the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors by writing the value of the index of the capacitor C_{n-1} to the destination capacitor C_k

index register. After that the process of charge transfer from the source capacitor C_i to the destination capacitor C_k is realized by the use of the current source I. This process is controlled by means of the control module CM on the basis of the output signals of the comparators K1 and K2 until the voltage U_i on the current source capacitor C_i observed by the use of the first comparator K1 equals zero during the period in which the function of the destination capacitor C_k is assigned to the capacitor C_0 having the lowest capacitance value in the array A of capacitors, or the voltage Uo, which increases on the capacitor C_0 and is simultaneously observed by the use of the second comparator K2, equals the reference voltage U_L value.

[0012] In the another variant of the method, after detecting the beginning of the active state of the signal on the trigger input InS by means of the control module CM, electric charge is delivered by the use of the current source I and accumulated in the sampling capacitor C_n, and at the same time the voltage U_n increasing on the sampling capacitor C_n is compared to the converted voltage U_{IN} value by the use of the second comparator K2. This process is realized until the voltage U_n, which increases on the sampling capacitor C_n equals the converted voltage U_{IN} value. After that, the function of the source capacitor C_i whose index is defined by the content of the source capacitor C_i index register in the control module CM is assigned by means of the control module CM to the sampling capacitor C_n by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register. At the same time, the function of the destination capacitor C_k, whose index is defined by the content of the destination capacitor C_k index register in the control module CM, is assigned by means of the control module CM to the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors by writing the value of the index of the capacitor C_{n-1} to the destination capacitor C_k index register. After that the process of electric charge transfer from the source capacitor C_i to the destination capacitor C_k is realized by the use of the current source I. This process is controlled by means of the control module CM on the basis of the output signals of the comparators K1 and K2 until the voltage U_i on the current source capacitor C_i observed by the use of the first comparator K1 equals zero during the period in which the function of the destination capacitor C_k is assigned to the capacitor C_0 having the lowest capacitance value in the array A of capacitors, or the voltage Uo, which increases on the capacitor C_0 and is simultaneously observed by the use of the second comparator K2, equals the reference voltage U_L value.

[0013] In the another variant of the method, after detecting the beginning of the active state of the signal on the trigger input InS by means of the control module CM, electric charge is delivered by the use of the current source I and accumulated in the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors and at the same time in the sampling capacitor C_n connected in parallel to the capacitor C_{n-1} in the array A of capacitors where the capacitance value of the sampling capacitor C_n is not smaller than the capacitance value of the capacitor C_{n-1}, and at the same time the voltage U_n increasing on the sampling capacitor C_n is compared to the converted voltage U_{IN} value by the use of the second comparator K2. This process is realized until the voltage U_n, which increases on the sampling capacitor C_n equals the converted voltage U_{IN} value, and after that the function of the source capacitor C_i, whose index is defined by the content of the source capacitor C_i index register in the control module CM, is assigned by means of the control module CM to the sampling capacitor C_n by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register. At the same time, the function of the destination capacitor C_k, whose index is defined by the content of the destination capacitor C_k index register in the control module CM, is assigned by means of the control module CM to the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors by writing the value of the index of the capacitor C_{n-1} to the destination capacitor C_k index register. After that, the process of charge transfer from the source capacitor C_i to the destination capacitor C_k is realized by the use of the current source I. This process is controlled by means of the control module CM on the basis of the output signals of the comparators K1 and K2 until the voltage U_i on the current source capacitor C_i observed by the use of the first comparator K1 equals zero during the period in which the function of the destination capacitor C_k is assigned to the capacitor C_0 having the lowest capacitance value in the array A of capacitors, or the voltage U_0, which increases on the capacitor C_0 and is simultaneously observed by the use of the second comparator K2, equals the reference voltage U_L value.

[0014] In the another variant of the method, after detecting the beginning of the active state of the signal on the trigger input InS by means of the control module CM, electric charge is delivered by the use of the current source I and accumulated in the sampling capacitor C_n, and at the same time the voltage U_n increasing on the sampling capacitor C_n is compared to the converted voltage U_{IN} value by the use of the second comparator K2. This process is realized until the voltage U_n, which increases on the sampling capacitor C_n equals the converted voltage U_{IN} value. After that, the function of the source capacitor C_i, whose index is defined by the content of the source capacitor C_i index register in the control module CM, is assigned by means of the control module CM to the sampling capacitor C_n by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register. At the same time, the function of the destination capacitor C_k, whose index is defined by the content of the destination capacitor C_k index register in the control module CM, is assigned by means of the control module CM to the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors by writing the value of the index of the capacitor C_{n-1} to the destination capacitor C_k index register. After that, the process of redistribution of accumulated charge is realized during which charge is transferred from the source capacitor C_i to the destination capacitor C_k by the use of the additional current source J

whose effectiveness is different from the effectiveness of the current source I. The process of charge redistribution is controlled by means of the control module CM on the basis of the output signals of the comparators K1 and K2 until the voltage U_i on the current source capacitor C_i observed by the use of the first comparator K1 equals zero during the period in which the function of the destination capacitor C_k is assigned to the capacitor C_0 having the lowest capacitance value in the array A of capacitors, or the voltage U_0, which increases on the capacitor C_0 and is simultaneously observed by the use of the second comparator K2, equals the reference voltage U_L value.

[0015] In the another variant of the method, after detecting the beginning of the active state of the signal on the trigger input InS by means of the control module CM, electric charge is delivered by the use of the current source I and accumulated in the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors and at the same time in the sampling capacitor C_n connected in parallel to the capacitor C_{n-1} in the array A of capacitors where the capacitance value of the sampling capacitor C_n is not smaller than the capacitance value of the capacitor C_{n-1}, and at the same time the voltage U_n increasing on the sampling capacitor C_n is compared to the converted voltage U_{IN} value by the use of the second comparator K2. This process is realized until the voltage U_n, which increases on the sampling capacitor C_n equals the converted voltage U_{IN} value. After that, the function of the source capacitor C_i, whose index is defined by the content of the source capacitor C_i index register in the control module CM, is assigned by means of the control module CM to the sampling capacitor C_n by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register. At the same time, the function of the destination capacitor C_k whose index is defined by the content of the destination capacitor C_k index register in the control module CM, is assigned by means of the control module CM to the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors by writing the value of the index of the capacitor C_{n-1} to the destination capacitor C_k index register. After that, the process of redistribution of accumulated charge is realized during which charge is transferred from the source capacitor C_i to the destination capacitor C_k by the use of the additional current source J whose effectiveness is different from the effectiveness of the current source I. The process of charge redistribution is controlled by means of the control module CM on the basis of the output signals of the comparators K1 and K2 until the voltage U_i on the current source capacitor C_i observed by the use of the first comparator K1 equals zero during the period in which the function of the destination capacitor C_k is assigned to the capacitor C_0 having the lowest capacitance value in the array A of capacitors, or the voltage U_0, which increases on the capacitor C_0 and is simultaneously observed by the use of the second comparator K2, equals the reference voltage U_L value.

[0016] The apparatus according to the invention (Fig. 1) comprises an array of capacitors with which the converted voltage U_{IN} and the set of control outputs E of the control module CM. The control module CM is equipped with the digital output B, the complete conversion signal output OutR, the trigger input InS and two control inputs In1 and In2 where the first control input In1 is connected to the output of the first comparator K1 whose inputs are connected to one pair of outputs of the array A of capacitors, and the other control input In2 of the control module CM is connected to the output of the second comparator K2 whose inputs are connected to the other pair of outputs of the array A. Furthermore, the source of auxiliary voltage U_H together with the source of the reference voltage U_L, the sampling capacitor C_n and the controlled current source I are connected to the array A of capacitors, and the control input of the current source I is connected to the control output A_I of the control module CM.

[0017] The array A in this variant of the apparatus (Fig. 3) comprises a number of n capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0, and a capacitance value of a capacitor of a given index is twice as high as a capacitance value of the capacitor of the previous index, while a relevant bit b_{n-1}, b_{n-2}, ..., b_1, b_0 in the digital output B of the control module CM is assigned to each capacitor C_{n-1}, C_{n-2}, ..., C_1, C_0. The sampling capacitor C_n is connected to the array A of capacitors, while the top plate of the sampling capacitor C_n is connected to the source of the converted voltage U_{IN} through the closed voltage source on-off switch S_{Un} and also it is connected through the closed first on-off switch S_{Ln} to the first rail L with which the top plates of all the capacitors C_n-$_1$, C_{n-2}, ..., C_1, C_0 in the array A of capacitors are connected through the open first on-off switches S_{Ln-1}, S_{Ln-2}, ..., SL1, S_{L0} in the array A. The top plate of the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors is also connected through the closed second on-off switch S_{Hn-1} in the array A to the second rail H with which the top plate of the sampling capacitor C_n is connected through the open second on-off switch S_{Hn} and with which the top plates of the other capacitors C_{n-2}, ..., C_1, C_0 in the array A are also connected through the open second on-off switches S_{Hn-2}, ..., S_{H1}, S_{H0} in the array A. The bottom plate of the sampling capacitor C_n is connected to the ground of the circuit through the change-over switch S_{Gn} whose moving contact is connected to its first stationary contact and the other stationary contact of the change-over switch S_{Gn} is connected to the source of auxiliary voltage U_H and also to the non-inverting input of the first comparator K1. The bottom plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A are connected to the source of auxiliary voltage U_H through the change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} in the array A whose moving contacts are connected to their other stationary contacts, and the first stationary contacts of the change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} in the array A are connected to the ground of the circuit (Fig. 3). The first rail L is connected to the ground of the circuit through the open first rail on-off switch S_{Gall} and to the non-inverting input of the second comparator K2 whose inverting input is connected to the source of the reference voltage U_L. The second rail H is connected to the inverting input of the first comparator K1. Moreover, the

control input of the first on-off switch S_{Ln} and the control inputs of the first on-off switches S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} in the array A and the control input of the change-over switch S_{Gn} and the control inputs of the relevant change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} in the array A are coupled together and connected to the relevant control outputs In and I_{n-1}, I_{n-2}, ..., I_1, I_0 of the set of control outputs E of the control module CM. The control input of the second on-off switch S_{Hn} and the control inputs of the second on-off switches S_{Hn-1}, S_{Hn-2}, ..., S_{H1}, S_{H0} in the array A and the control input of the first rail on-off switch S_{Gall} are connected to the relevant control outputs D_n, D_{n-1}, D_{n-2}, ..., D_1, D_0 and D_{all} of the set of control outputs E of the control module CM (Fig. 3). One end of the current source I is connected to the second rail H, and the other end of the current source I is connected to the first rail L. The control input of the current source I is connected to the control output A_I of the control module CM. The control input of the voltage source on-off switch S_{Un} is connected to the control output A_U of the control module CM.

[0018] In the another version of this apparatus variant (Fig. 7) the sampling capacitor C_n is connected in parallel to the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors while the capacitance value of the sampling capacitor C_n is not smaller than the capacitance value of the capacitor C_{n-1}. At the same time, both capacitors C_n and C_{n-1} are connected in parallel to the source of the converted voltage U_{IN} in a way that the top plate of the capacitor C_{n-1} in the array A of capacitors is connected to the source of the converted voltage U_{IN} through the closed additional voltage source on-off switch S_{Un-1}, and the bottom plate of the capacitor C_{n-1} is connected to the ground of the circuit through the change-over switch S_{Gn-1} in the array A whose moving contact is connected to its first stationary contact, and the other stationary contact of the change-over switch S_{Gn-1} in the array A is connected to the source of auxiliary voltage U_H. Moreover, the top plate of the capacitor C_{n-1} in the array A of capacitors is connected also to the first rail L through the closed first on-off switch S_{Ln-1} in the array A. The control input of the voltage source on-off switch S_{Un} and the control input of the additional voltage source on-off switch S_{Un-1} are coupled together and connected to the control output A_U of the control module CM,

[0019] In the another variant of the apparatus (Fig. 8), a voltage supply U_{DD} is additionally connected to the array A of capacitors.

[0020] The array A in this variant of the apparatus (Fig. 10) comprises a number of n capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0, and a capacitance value of a capacitor of a given index is twice as high as a capacitance value of the capacitor of the previous index, while a relevant bit b_{n-1}, b_{n-2}, ..., b_1, b_0 in the digital output B of the control module CM is assigned to each capacitor C_{n-1}, C_{n-2}, ..., C_1, C_0. The sampling capacitor C_n is connected to the array A of capacitors, while the top plate of the sampling capacitor C_n is connected through the closed first on-off switch S_{Ln} to the first rail L with which also the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A of capacitors are connected through the open first on-off switches S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} in the array A. The top plate of the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors is connected through the closed second on-off switch S_{Hn-1} in the array A to the second rail H with which the top plate of the sampling capacitor C_n is also connected through the open second on-off switch S_{Hn} and with which the top plates of the other capacitors C_{n-2}, ..., C_1, C_0 in the array A are connected through the open second on-off switches S_{Hn-2}, ..., S_{H1}, S_{H0} in the array A. The bottom plate of the sampling capacitor C_n is connected to the ground of the circuit through the change-over switch S_{Gn} whose moving contact is connected to its first stationary contact and the other stationary contact of the change-over switch S_{Gn} is connected to the source of auxiliary voltage U_H and also to the non-inverting input of the first comparator K1. The bottom plates of all the capacitors C_{n-1}, Cn-2, ..., C_1, C_0 in the array A are connected to the source of auxiliary voltage U_H through the change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} in the array A whose moving contacts are connected to their other stationary contacts, and the first stationary contacts of the change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} in the array A are connected to the ground of the circuit (Fig. 10). The first rail L is connected to the ground of the circuit through the open first rail on-off switch S_{Gall} and to the non-inverting input of the second comparator K2 whose inverting input is connected to the source of the converted voltage U_{IN} through the voltage source change-over switch Su whose moving contact is connected to its first stationary contact and the other stationary contact of the voltage source change-over switch Su is connected to the source of the reference voltage U_L, while the second rail H is connected to the inverting input of the first comparator K1. The control input of the first on-off switch S_{Ln} and the control inputs of the first on-off switches S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} in the array A and the control input of the change-over switch S_{Gn} and the control inputs of the relevant change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} in the array A are coupled together and connected to the relevant control outputs I_n and I_{n-1}, I_{n-2}, ..., I_1, I_0 of the set of control outputs E of the control module CM. The control input of the second on-off switch S_{Hn} and the control inputs of the second on-off switches S_{Hn-1}, S_{Hn-2}, ..., S_{H1}, S_{H0} in the array A and the control input of the first rail on-off switch S_{Gall} are connected to the relevant control outputs D_n, D_{n-1}, D_{n-2}, ..., D_1, D_0 and D_{all} of the set of control outputs E of the control module CM. The control input of the voltage source change-over switch Su is connected to the control output A_U of the control module CM (Fig. 10). One end of the current source I is connected to the voltage supply U_{DD} through the current source change-over switch S_I whose moving contact is connected to its first stationary contact and the other stationary contact of the current source change-over switch S_I is connected to the second rail H. The other end of the current source I is connected to the first rail L. Moreover, the control input of the current source change-over switch S_I is connected to the control output As of the control module CM, and the control

input of the current source I is connected to the control output A_I of the control module CM.

[0021] In the another version of this apparatus variant (Fig. 13), the sampling capacitor C_n, whose capacitance value is not smaller than the capacitance value of the capacitor C_{n-1}, is connected in parallel to the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors through the first rail L and through the ground of the circuit in a way that the top plate of the capacitor C_{n-1} in the array A of capacitors is connected to the first rail L through the closed first on-off switch S_{Ln-1} in the array A, and the bottom plate of the capacitor C_{n-1} is connected to the ground of the circuit through the change-over switch S_{Gn-1} in the array A whose moving contact is connected to its first stationary contact, and the other stationary contact of the change-over switch S_{Gn-1} in the array A is connected to the source of auxiliary voltage U_H.

[0022] In the another variant of the apparatus (Fig. 14), the voltage supply U_{DD} and a controlled additional current source J are connected to the array A of capacitors, and the control input of the additional current source J is connected to the control output A_J of the control module CM.

[0023] The array A in this variant of the apparatus (Fig. 16) comprises a number of n capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0, and a capacitance value of a capacitor of a given index is twice as high as a capacitance value of the of the previous index, while a relevant bit b_{n-1}, b_{n-2}, ..., b_1, b_0 in the digital output B of the control module CM is assigned to each capacitor C_{n-1}, C_{n-2}, ..., C_1, C_0. The sampling capacitor C_n is connected to the array A of capacitors, while the top plate of the sampling capacitor C_n is connected through the closed first on-off switch S_{Ln} to the first rail L with which also the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A of capacitors are connected through the open first on-off switches S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} in the array A. The top plate of the sampling capacitor C_n is also connected through the closed second on-off switch S_{Hn} to the second rail H with which the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A are connected through the open second on-off switches S_{Hn-1}, S_{Hn-2}, ..., S_{H1}, S_{H0} in the array A. The bottom plate of the sampling capacitor C_n is connected to the ground of the circuit through the change-over switch S_{Gn} whose moving contact is connected to its first stationary contact and the other stationary contact of the change-over switch S_{Gn} is connected to the source of auxiliary voltage U_H and also to the non-inverting input of the first comparator K1. The bottom plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A are connected to the source of auxiliary voltage U_H through the change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} in the array A whose moving contacts are connected to their other stationary contacts, and the first stationary contacts of the change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} in the array A are connected to the ground of the circuit (Fig. 16). The first rail L is connected to the ground of the circuit through the open first rail on-off switch S_{Gall} and to the non-inverting input of the second comparator K2 whose inverting input is connected to the source of the converted voltage U_{IN} through the voltage source change-over switch S_U whose moving contact is connected to its first stationary contact and the other stationary contact of the voltage source change-over switch S_U is connected to the source of the reference voltage U_L. The second rail H is connected to the inverting input of the first comparator K1. Moreover, the control input of the first on-off switch S_{Ln} and the control inputs of the first on-off switches S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} in the array A and the control input of the change-over switch S_{Gn} and the control inputs of the relevant change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} in the array A are coupled together and connected to the relevant control outputs I_n and I_{n-1}, I_{n-2}, ..., I_1, I_0 of the set of control outputs E of the control module CM. The control input of the second on-off switch S_{Hn} and the control inputs of the second on-off switches S_{Hn-1}, S_{Hn-2}, ..., S_{H1}, S_{H0} in the array A and the control input of the first rail on-off switch S_{Gall} are connected to the relevant control outputs D_n, D_{n-1}, D_{n-2}, ..., D_1, D_0 and D_{all} of the set of control outputs E of the control module CM. The control input of the voltage source change-over switch Su is connected to the control output A_U of the control module CM (Fig. 16). One end of the current source I is connected to the voltage supply U_{DD}. The other end of the current source I is connected to the first rail L, with which also the other end of the additional current source J is connected. One end of the additional current source J is connected to the second rail H. The control input of the current source I is connected to the control output A_I of the control module CM while the control input of the additional current source J is connected to the control output A_J of the control module CM.

[0024] In the another version of this apparatus variant (Fig. 19), the sampling capacitor C_n whose capacitance value is not smaller than the capacitance value of the capacitor C_{n-1}, is connected in parallel to the capacitor C_{n-1} having the highest capacitance value in the array A of capacitors through the first rail L and through the ground of the circuit in a way that the top plate of the capacitor C_{n-1} in the array A of capacitors is connected to the first rail L through the closed first on-off switch S_{Ln-1} in the array A, and the bottom plate of the capacitor C_{n-1} is connected to the ground of the circuit through the change-over switch S_{Gn-1} in the array A whose moving contact is connected to its first stationary contact, and the other stationary contact of the change-over switch S_{Gn-1} in the array A is connected to the source of auxiliary voltage U_H.

[0025] The apparatus according to the invention operates as follows.

Between successive cycles of conversion of voltage values to digital words having a number of bits equal to n, the control module CM keeps the apparatus in the state of relaxation during which the control module CM causes, by means of the control signals provided on the outputs I_n and I_{n-1}, I_{n-2}, ..., I_1, I_0, the closure of the first on-off switches S_{Ln} and S_{Ln-1}, S_{Ln-2},..., S_{L1}, S_{L0} and thereby the connection of the top plate of the sampling capacitor C_n and of the top plates of all

the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A to the first rail L, and also the switching of the change-over switches S_{Gn}, S_{Gn-1},..., S_{G1}, S_{G0} and thereby the connection of the bottom plate of the sampling capacitor C_n and also the connection of the bottom plates of the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A to the ground of the circuit. On the other hand, by means of the control signal provided on the output D_{all}, the control module CM causes the closure of the first rail on-off switch S_{Gall} and thereby the connection of the first rail L to the ground of the circuit enforcing in this way a complete discharge of the sampling capacitor C_n and of the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A. Afterwards, the control module CM causes, by means of the control signal provided on the output D_{n-1}, the closure of the second on-off switch S_{Hn-1} and thereby the connection of the second rail H to the first rail L and to the ground of the circuit which prevents the occurrence of a random potential on the second rail H. At the same time, the control module CM causes, by means of the control signals provided on the output A_U, the opening of the voltage source on-off switch S_{Un} and thereby the disconnection of the top plate of the sampling capacitor C_n from the source of the converted voltage U_{IN}. At the same time, the control module CM causes, by means of the control signals provided on the output D_n and on the outputs D_{n-2}, ..., D_1, D_0, the opening of the second on-off switches S_{Hn} and S_{Hn-2}, ..., S_{H1}, S_{H0}. At the same time, the control module CM causes, by means of the control signal provided on the output A_I, the switching off the current source I (Fig. 2). As soon as the control module CM detects the beginning of the active state of the signal on the trigger input InS of the apparatus, the control module CM causes, by means of the control signal provided on the output D_{all}, the opening of the first rail on-off switch S_{Gall} and thereby the disconnection of the first rail L from the ground of the circuit. At the same time, the control module CM causes, by means of the control signals provided on the outputs I_{n-1}, I_{n-2}, ..., I_1, I_0, the opening of the first on-off switches S_{Ln-1}, S_{Ln-2},..., S_{L1}, S_{L0} and thereby the disconnection of the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A from the first rail L, and also the switching of the change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} and thereby the connection of the bottom plates of the capacitors C_{n-1}, C_{n-2},..., C_1, C_0 to the source of auxiliary voltage U_H. At the same time, by means of the control signal provided on the output A_U, the control module CM causes the closure of the voltage source on-off switch S_{Un} and thereby the connection of the top plate of the sampling capacitor C_n to the source of the converted voltage U_{IN} (Fig. 3). At the same time, the control module CM deactivates the signal provided on the complete conversion signal output OutR and assigns the initial value zero to all the bits b_{n-1}, b_{n-2}, ..., b_1, b_0 in the digital word. The electric charge is accumulated in the sampling capacitor C_n during the active state of the signal on the trigger input InS of the apparatus while the sampling capacitor C_n is the only capacitor connected at that time to the source of the converted voltage U_{IN} through the closed voltage source on-off switch S_{Un} and through the ground of the circuit. The electric charge accumulated in the sampling capacitor C_n during the active state of the signal on the trigger input InS of the apparatus produces a voltage U_n whose value is proportional to the converted voltage U_{IN} value.

When the control module CM detects the end of the active state of the signal on the trigger input InS of the apparatus, the control module CM causes, by means of the control signal provided on the output A_U, the opening of the voltage source on-off switch S_{Un} and thereby the disconnection of the top plate of the sampling capacitor C_n from the source of the converted voltage U_{IN}. At the same time, the control module CM causes, by means of the control signal provided on the output I_n, the opening of the first on-off switch S_{Ln} and thereby the disconnection of the top plate of the sampling capacitor C_n from the first rail L, and also the concurrent switching of the change-over switch S_{Gn} and thereby the connection of the bottom plate of the sampling capacitor C_n to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signal provided on the output D_{n-1}, the opening of the second on-off switch S_{Hn-1} and thereby the disconnection of the top plate of the capacitor C_{n-1} from the second rail H. Next, by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register in the control module CM, the control module CM assigns the function of the source capacitor C_i, whose index is defined by the content of the source capacitor C_i index register, to the sampling capacitor C_n. At the same time, the control module CM causes, by means of the control signal provided on the output D_i, the closure of the second on-off switch S_{Hi} and thereby the connection of the top plate of the source capacitor C_i to the second rail H. At the same time, by writing the value of the index of the capacitor C_{n-1} having the highest capacitance value in the array A to the destination capacitor C_k index register in the control module CM, the control module CM assigns the function of the destination capacitor C_k whose index is defined by the content of the destination capacitor C_k index register to the capacitor C_{n-1}. Then, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of the destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit. Then, by means of the control signal provided on the output A_I, the control module CM causes the switching on the current source I by the use of which the charge accumulated in the source capacitor C_i is transferred through the second rail H and through the first rail L to the destination capacitor C_k (Fig. 4) while the voltage U_i on the source capacitor C_i progressively decreases whereas at the same time the voltage U_k on the destination capacitor C_k progressively increases.

In case when the voltage U_k on the current destination capacitor C_k reaches the reference voltage U_L value during the charge transfer, the control module CM on the basis of the output signal of the second comparator K2 assigns the value

one to the relevant bit b_k in the digital word, and the control module CM causes, by means of the control signal provided on the output I_k, the opening of the first on-off switch S_{Lk} and thereby the disconnection of the top plate of the destination capacitor C_k from the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the source of auxiliary voltage U_H. Afterwards, by reduction of the content of the destination capacitor C_k index register by one, the control module CM assigns the function of the destination capacitor C_k to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before. After that, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of a new destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit.

In case when the voltage U_i on the source capacitor C_i reaches the value zero during the charge transfer, the control module CM, on the basis of the output signal of the first comparator K1 causes, by means of the control signal provided on the output D_i, the opening of the second on-off switch S_{Hi} and thereby the disconnection of the top plate of the source capacitor C_i from the second rail H. At the same time, the control module CM causes, by means of the control signal provided on the output I_k, the opening of the first on-off switch S_{Lk} and thereby the disconnection of the top plate of the destination capacitor C_k from the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the source of auxiliary voltage U_H. Next, the control module CM, on the basis of the output signal of the first comparator K1 by writing the current content of the destination capacitor C_k index register to the source capacitor C_i index register, assigns the function of the source capacitor C_i to the capacitor that until now has acted as the destination capacitor C_k, and after that the control module CM causes, by means of the control signal provided on the output D_i, the closure of the second on-off switch S_{Hi} and thereby the connection of the top plate of a new source capacitor C_i to the second rail H. Afterwards, by reduction of the content of the destination capacitor C_k index register by one, the control module CM assigns the function of the destination capacitor C_k, whose index is defined by the content of the destination capacitor C_k index register in the control module CM, to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before. After that, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of the capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the new destination capacitor C_k to the ground of the circuit (Fig. 5).

In both cases the control module CM continues to control the process of charge transfer on the basis of the output signals of both comparators K1 and K2. Each occurrence of the active state on the output of second comparator K2 causes the assignment of the function of the destination capacitor C_k to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before. On the other hand, each occurrence of the active state on the output of first comparator K1 causes the assignment of the function of the source capacitor C_i to the capacitor that until now has acted as the destination capacitor C_k, and at the same time the assignment of the function of the destination capacitor C_k to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before.

The process of charge redistribution is terminated when the capacitor C_0 having the lowest capacitance value in the array A stops to act as the destination capacitor C_k. Such situation occurs when the active state appears on the output of the first comparator K1 or on the output of the second comparator K2 during charge transfer to the capacitor C_0. When the active state appears on the output of the second comparator K2, the control module CM assigns the value one to the bit b_0.

After termination of redistribution of charge accumulated previously in the sampling capacitor C_n and after assigning the corresponding values to the bits b_{n-1}, b_{n-2}, ..., b_1, b_0 in the output digital word, the control module CM activates the signal provided on the complete conversion signal output OutR and causes introduction of the apparatus into the relaxation phase by switching off the current source I, the opening of the voltage source on-off switch S_{Un} and thereby the disconnection of the top plate of the sampling capacitor C_n from the source of the converted voltage U_{IN}, also the closure of the first on-off switches S_{Ln} and S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} and thereby the connection of the top plate of the sampling capacitor C_n and the connection of the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A to the first rail L, and also the concurrent switching of the change-over switches S_{Gn} and S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} to the positions connecting the bottom plate of the sampling capacitor C_n and the bottom plates of the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 to the ground of the circuit. At the same time, the control module causes the closure of the first rail on-off switch S_{Gall} and thereby the connection of the first rail L to the ground of the circuit, enforcing a complete discharge of the sampling capacitor C_n and of the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A, and also the opening of the second on-off switches S_{Hn} and S_{Hn-2}, ..., S_{H1}, S_{H0} in the array A, and also the closure of the second on-off switch S_{Hn-1} and thereby the connection of the second rail H to the first rail L and to the ground of the circuit (Fig. 2), which prevents the occurrence

of a random potential on the first rail H.

[0026] The operation of the another version of this apparatus variant consists in that during the time when the apparatus is kept in the state of relaxation, the control module CM causes, by means of the control signals provided on the output A_U, the opening of the voltage source on-off switch S_{Un} and thereby the disconnection of the top plate of the sampling capacitor C_n from the source of the converted voltage U_{IN}, and also the opening of the additional voltage source on-off switch S_{Un-1} and thereby the disconnection of the top plate of the capacitor C_{n-1} having the highest capacitance value in the array A from the source of the converted voltage U_{IN} (Fig. 6). As soon as the control module CM detects the beginning of the active state of the signal on the trigger input InS of the apparatus, the control module CM causes, by means of the control signal provided on the output D_{all}, the opening of the first rail on-off switch S_{Gall} and thereby the disconnection of the first rail L from the ground of the circuit. At the same time, the control module CM causes, by means of the control signals provided on the outputs I_{n-2}, ..., I_1, I_0, the opening of the first on-off switches S_{Ln-2},..., S_{L1}, S_{L0} and thereby the disconnection of the top plates of all the capacitors C_{n-2}, ..., C_1, C_0 in the array A from the first rail L and also the switching of the change-over switches S_{Gn-2}, ..., S_{G1}, S_{G0} and thereby the connection of the bottom plates of the capacitors C_{n-2},..., C_1, C_0 to the source of auxiliary voltage U_H. At the same time, by means of the control signal provided on the output A_U, the control module CM causes the closure of the voltage source on-off switch S_{Un} and thereby the connection of the top plate of the sampling capacitor C_n to the source of the converted voltage U_{IN}, and also the closure of the additional voltage source on-off switch S_{Un-1} and thereby the connection of the top plate of the capacitor C_{n-1} in the array A of capacitors to the source of the converted voltage U_{IN} (Fig. 7). At the same time, the control module CM deactivates the signal provided on the complete conversion signal output OutR and assigns the initial value zero to all the bits b_{n-1}, b_{n-2}, ..., b_1, b_0 in the digital word. The electric charge is accumulated in the capacitor C_{n-1} and at the same time in the sampling capacitor C_n connected in parallel to the capacitor C_{n-1} in the array A of capacitors which are the only capacitors connected at that time to the source of the converted voltage U_{IN} through the closed voltage source on-off switch S_{Un} and through the closed additional voltage source on-off switch S_{Un-1} and through the ground of the circuit. When the control module CM detects the end of the active state of the signal on the trigger input InS of the apparatus, the control module CM causes, by means of the control signal provided on the output A_U, the opening of the voltage source on-off switch S_{Un} and thereby the disconnection of the top plate of the sampling capacitor C_n from the source of the converted voltage U_{IN}, and also the concurrent opening of the additional voltage source on-off switch S_{Un-1} and thereby the disconnection of the top plate of the capacitor C_{n-1} from the source of the converted voltage U_{IN}. At the same time, the control module CM causes by means of the control signal provided on the output I_n, the opening of the first on-off switch S_{Ln} and thereby the disconnection of the top plate of the sampling capacitor C_n from the first rail L, and also the concurrent switching of the change-over switch S_{Gn} and thereby the connection of the bottom plate of the sampling capacitor C_n to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signal provided on the output D_{n-1}, the opening of the second on-off switch S_{Hn-1} and thereby the disconnection of the top plate of the capacitor C_{n-1} from the second rail H. Next, by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register in the control module CM, the control module CM assigns the function of the source capacitor C_i, whose index is defined by the content of the source capacitor C_i index register, to the sampling capacitor C_n. At the same time, the control module CM causes, by means of the control signal provided on the output D_i, the closure of the second on-off switch S_{Hi}, and thereby the connection of the top plate of the source capacitor C_i to the second rail H. At the same time, by writing the value of the index of the capacitor C_{n-1} having the highest capacitance value in the array A to the destination capacitor C_k index register in the control module CM, the control module CM assigns the function of the destination capacitor C_k, whose index is defined by the content of the destination capacitor C_k index register, to the capacitor C_{n-1}. Then, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of the destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit. Then, by means of the control signal provided on the output A_I, the control module CM causes the switching on the current source I by the use of which the charge accumulated in the source capacitor C_i is transferred through the second rail H and through the first rail L to the destination capacitor C_k. Next, the control module CM starts to control the process of redistribution of accumulated charge that is terminated when the capacitor Co having the lowest capacitance value in the array A stops to act as the destination capacitor C_k. After that the control module CM activates the signal provided on the complete conversion signal output OutR, and causes introducing the apparatus into the relaxation phase again.

[0027] The another variant of the apparatus operates as follows. Between successive cycles of conversion of voltage values to digital words having a number of bits equal to n, the control module CM keeps the apparatus in the state of relaxation during which the control module CM causes, by means of the control signals provided on the outputs In and I_{n-1},..., I_1, I_0, the closure of the first on-off switches S_{Ln} and S_{Ln-1},..., S_{L1}, S_{L0} and thereby the connection of the top plate of the sampling capacitor C_n and the connection of the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A to the first rail L, and also the switching of the change-over switches S_{Gn}, S_{Gn-1},..., S_{G1}, S_{G0} and thereby the connection of the bottom plate of the sampling capacitor C_n and the connection of the bottom plates of the capacitors C_{n-1}, ..., C_1,

C_0 in the array A to the ground of the circuit. On the other hand, by means of the control signal provided on the output D_{all}, the control module CM causes the closure of the first rail on-off switch S_{Gall} and thereby the connection of the first rail L to the ground of the circuit enforcing in this way a complete discharge of the sampling capacitor C_n and of the capacitors C_{n-1}, ..., C_1, C_0 in the array A. Afterwards, the control module CM causes, by means of the control signal provided on the output D_{n-1}, the closure of the second on-off switch S_{Hn-1} and thereby the connection of the second rail H to the first rail L and to the ground of the circuit which prevents the occurrence of a random potential on the second rail H. At the same time, the control module CM causes, by means of the control signals provided on the output A_U, the switching of the voltage source change-over switch Su and thereby the connection of the inverting input of the second comparator K2 to the source of the reference voltage U_L. At the same time, the control module CM causes, by means of the control signals provided on the output D_n and on the outputs D_{n-2}, ..., D1, D_0, the opening of the second on-off switches S_{Hn} and S_{Hn-2}, ..., S_{H1}, S_{H0}. At the same time, the control module CM causes, by means of the control signal provided on the output A_I, the switching off the current source I, and on the other hand, by means of the control signal provided on the output A_S, the switching of the current source change-over switch S_I and thereby the connection of the one end of the current source I to the voltage supply U_{DD} (Fig. 9).

As soon as the control module CM detects the beginning of the active state of the signal on the trigger input InS of the apparatus, the control module CM causes, by means of the control signal provided on the output A_U, the switching of the voltage source change-over switch S_U and thereby the connection of the inverting input of the second comparator K2 to the source of the converted voltage U_{IN}. At the same time, the control module CM causes, by means of the control signal provided on the output D_{all}, the opening of the first rail on-off switch S_{Gall} and thereby the disconnection of the first rail L from the ground of the circuit. At the same time, the control module CM causes, by means of the control signals provided on the outputs I_{n-1}, I_{n-2}, ..., I_1, I_0, the opening of the first on-off switches S_{Ln-1}, S_{Ln-2},..., S_{L1}, S_{L0} and thereby the disconnection of the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A from the first rail L and also the switching of the change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} and thereby the connection of the bottom plates of the capacitors C_{n-1}, C_{n-2},..., C_1, C_0 to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signal provided on the output A_I, the switching on the current source I (Fig. 10). At the same time, the control module CM deactivates the signal provided on the complete conversion signal output OutR and assigns the initial value zero to all the bits b_{n-1}, b_{n-2}, ..., b_1, b_0 in the digital word. The electric charge delivered by the use of the current source I is accumulated in the sampling capacitor C_n which is the only capacitor connected at that time to the other end of the current source I through the first rail L and through the closed first on-off switch S_{Ln}. Accumulation of charge in the sampling capacitor C_n causes a progressive increase of the voltage U_n on that capacitor which is compared by the second comparator K2 to the converted voltage U_{IN} value.

When the voltage U_n increasing on the sampling capacitor C_n reaches the converted voltage U_{IN} value which represents the mapping of the converted voltage U_{IN} value to the portion of electric charge proportional to this value and accumulated in the sampling capacitor C_n, the control module CM on the basis of the output signal of the second comparator K2 causes, by means of the control signal provided on the output I_n, the opening of the first on-off switch S_{Ln} and thereby the disconnection of the top plate of the sampling capacitor C_n from the first rail L, and also the concurrent switching of the change-over switch S_{Gn} and thereby the connection of the bottom plate of the sampling capacitor C_n to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signal provided on the output D_{n-1}, the opening of the second on-off switch S_{Hn-1} and thereby the disconnection of the top plate of the capacitor C_{n-1} from the second rail H. At the same time, the control module CM causes, by means of the control signals provided on the output A_U, the switching of the voltage source change-over switch Su and thereby the connection of the inverting input of the second comparator K2 to the source of the reference voltage U_L. Next, the control module CM causes, by means of the control signal provided on the output As, the switching of the current source change-over switch S_I and thereby the connection of the one end of the current source I to the second rail H. Next, by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register in the control module CM, the control module CM assigns the function of the source capacitor C_i whose index is defined by the content of the source capacitor C_i index register to the sampling capacitor C_n. At the same time, the control module CM causes, by means of the control signal provided on the output D_i, the closure of the second on-off switch S_{Hi} and thereby the connection of the top plate of the source capacitor C_i to the second rail H. At the same time, by writing the value of the index of the capacitor C_{n-1} having the highest capacitance value in the array A to the destination capacitor C_k index register in the control module CM, the control module CM assigns the function of the destination capacitor C_k whose index is defined by the content of the destination capacitor C_k index register to the capacitor C_{n-1}. Then, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of the destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit. Afterwards, the charge accumulated in the source capacitor C_i is transferred through the second rail H and through the first rail L to the destination capacitor C_k (Fig. 4) while the voltage U_i on the source capacitor C_i progressively decreases whereas at the same time the voltage U_k on the destination capacitor C_k progressively increases.

In case when the voltage U_k on the current destination capacitor C_k reaches the reference voltage U_L value during the charge transfer, the control module CM on the basis of the output signal of the second comparator K2 assigns the value one to the relevant bit b_k in the digital word, and the control module CM causes, by means of the control signal provided on the output I_k, the opening of the first on-off switch S_{Lk} and thereby the disconnection of the top plate of the destination capacitor C_k from the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the source of auxiliary voltage U_H. Afterwards, by reduction of the content of the destination capacitor C_k index register by one, the control module CM assigns the function of the destination capacitor C_k to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before. After that, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of a new destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit.

In case when the voltage U_i on the source capacitor C_i reaches the value zero during the charge transfer, the control module CM, on the basis of the output signal of the first comparator K1 causes, by means of the control signal provided on the output D_i, the opening of the second on-off switch S_{Hi} and thereby the disconnection of the top plate of the source capacitor C_i from the second rail H. At the same time, the control module CM causes, by means of the control signal provided on the output I_k, the opening of the first on-off switch S_{Lk} and thereby the disconnection of the top plate of the destination capacitor C_k from the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the source of auxiliary voltage U_H. Next, the control module CM, on the basis of the output signal of the first comparator K1 by writing the current content of the destination capacitor C_k index register to the source capacitor C_i index register, assigns the function of the source capacitor C_i to the capacitor that until now has acted as the destination capacitor C_k, and after that, the control module CM causes, by means of the control signal provided on the output D_i, the closure of the second on-off switch S_{Hi} and thereby the connection of the top plate of a new source capacitor C_i to the second rail H. Afterwards, by reduction of the content of the destination capacitor C_k index register by one, the control module CM assigns the function of the destination capacitor C_k, whose index is defined by the content of the destination capacitor C_k index register in the control module CM, to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before. Then, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of the destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit (Fig. 5).

In both cases, the control module CM continues to control the process of charge transfer on the basis of the output signals of both comparators K1 and K2. Each occurrence of the active state on the output of second comparator K2 causes the assignment of the function of the destination capacitor C_k to the subsequent capacitor in the array A, whose capacitance value is twice as lower as the capacitance value of the capacitor, which acted as the destination capacitor directly before. On the other hand, each occurrence of the active state on the output of first comparator K1 causes the assignment of the function of the source capacitor C_i to the capacitor that until now has acted as the destination capacitor C_k, and at the same time the assignment of the function of the destination capacitor C_k to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before.

The process of charge redistribution is terminated when the capacitor C_0 having the lowest capacitance value in the array A stops to act as the destination capacitor C_k. Such situation occurs when the active state appears on the output of the first comparator K1 or on the output of the second comparator K2 during charge transfer to the capacitor C_0. When the active state appears on the output of the second comparator K2, the control module CM assigns the value one to the bit b_0.

After termination of redistribution of charge delivered by the use of the current source I and accumulated previously in the sampling capacitor C_n and after assigning the corresponding values to the bits b_{n-1}, b_{n-2}, ..., b_1, b_0 in the output digital word, the control module CM activates the signal provided on the complete conversion signal output OutR and causes introduction of the apparatus into the relaxation phase by switching off the current source I, also the switching of the current source change-over switch S_I and thereby the connection of the one end of the current source I to the voltage supply U_{DD}, also the switching of the voltage source change-over switch S_U to the position connecting the inverting input of the second comparator K2 to the source of the reference voltage U_L, also the closure of the first on-off switches S_{Ln} and S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} and thereby the connection of the top plate of the sampling capacitor C_n and the connection of the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A to the first rail L, and also the concurrent switching of the change-over switches S_{Gn} and S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} to the positions connecting the bottom plate of the sampling capacitor C_n and the bottom plates of the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 to the ground of the circuit. At the same time, the control module causes the closure of the first rail on-off switch S_{Gall} and thereby the

connection of the first rail L to the ground of the circuit, enforcing a complete discharge of the sampling capacitor C_n and of the capacitors C_{n-1}, C_{n-2}, ..., C_1, C_0 in the array A, and also the opening of the second on-off switches S_{Hn} and S_{Hn-2}, ..., S_{H1}, S_{H0} in the array A, and also the closure of the second on-off switch S_{Hn-1} and thereby the connection of the second rail H to the first rail L and to the ground of the circuit (Fig. 9) which prevents the occurrence of a random potential on the first rail H.

[0028] The operation of the another version of this apparatus variant consists in that as soon as the control module CM detects the beginning of the active state of the signal on the trigger input InS of the apparatus, the control module CM causes, by means of the control signal provided on the output A_U, the switching of the voltage source change-over switch S_U and thereby the connection of the inverting input of the second comparator K2 to the source of the converted voltage U_{IN}. At the same time, the control module CM causes, by means of the control signal provided on the output D_{all}, the opening of the first rail on-off switch S_{Gall} and thereby the disconnection of the first rail L from the ground of the circuit. At the same time, the control module CM causes, by means of the control signals provided on the outputs I_{n-2}, ..., I_1, I_0, the opening of the first on-off switches S_{Ln-2},..., S_{L1}, S_{L0} and thereby the disconnection of the top plates of all the capacitors C_{n-2}, ..., C_1, Co in the array A from the first rail L and also the switching of the change-over switches S_{Gn-2}, ..., S_{G1}, S_{G0} and thereby the connection of the bottom plates of the capacitors C_{n-2},..., C_1, Co to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signal provided on the output A_I, the switching on the current source I (Fig. 13). At the same time, the control module CM deactivates the signal provided on the complete conversion signal output OutR and assigns the initial value zero to all the bits b_{n-1}, b_{n-2}, ..., b_1, bo in the digital word. The electric charge is accumulated in the capacitor C_{n-1} and at the same time in the sampling capacitor C_n connected in parallel to the capacitor C_{n-1} in the array A of capacitors which are the only capacitors connected at that time to the other end of the current source I through the first rail L and through the closed first on-off switches S_{Ln} and S_{Ln-1}.

When the voltage U_n increasing on the sampling capacitor C_n reaches the converted voltage U_{IN} value, the control module CM on the basis of the output signal of the second comparator K2 causes, by means of the control signal provided on the output In, the opening of the first on-off switch S_{Ln} and thereby the disconnection of the top plate of the sampling capacitor C_n from the first rail L, and also the concurrent switching of the change-over switch S_{Gn} and thereby the connection of the bottom plate of the sampling capacitor C_n to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signal provided on the output D_{n-1}, the opening of the second on-off switch S_{Hn-1} and thereby the disconnection of the top plate of the capacitor C_{n-1} from the second rail H, and on the other hand, by means of the control signals provided on the output A_U, the switching of the voltage source change-over switch Su and thereby the connection of the inverting input of the second comparator K2 to the source of the reference voltage U_L. Next, the control module CM causes, by means of the control signal provided on the output As, the switching of the current source change-over switch S_I and thereby the connection of the one end of the current source I to the second rail H. Next, by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register in the control module CM, the control module CM assigns the function of the source capacitor C_i whose index is defined by the content of the source capacitor C_i index register to the sampling capacitor C_n. At the same time, the control module CM causes, by means of the control signal provided on the output D_i, the closure of the second on-off switch S_{Hi} and thereby the connection of the top plate of the source capacitor C_i to the second rail H. At the same time, by writing the value of the index of the capacitor C_{n-1} having the highest capacitance value in the array A to the destination capacitor C_k index register in the control module CM, the control module CM assigns the function of the destination capacitor C_k whose index is defined by the content of the destination capacitor C_k index register to the capacitor C_{n-1}. Then, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of the destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit. Afterwards, the charge accumulated in the source capacitor C_i is transferred through the second rail H and through the first rail L to the destination capacitor C_k (Fig. 11). Next, the control module CM starts to control the process of redistribution of accumulated charge that is terminated when the capacitor Co having the lowest capacitance value in the array A stops to act as the destination capacitor C_k. After that the control module CM activates the signal provided on the complete conversion signal output OutR, and causes introducing the apparatus into the relaxation phase again.

[0029] The another variant of the apparatus operates as follows. Between successive cycles of conversion of voltage values to digital words having a number of bits equal to n, the control module CM keeps the apparatus in the state of relaxation during which the control module CM causes, by means of the control signals provided on the outputs In and I_{n-1}, I_{n-2}, ..., I_1, I_0, the closure of the first on-off switches S_{Ln} and S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} and thereby the connection of the top plate of the sampling capacitor C_n and the connection of the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, Co in the array A to the first rail L, and also the switching of the change-over switches S_{Gn} and S_{Gn-1},..., S_{G1}, S_{G0} and thereby the connection of the bottom plate of the sampling capacitor C_n and the connection of the bottom plates of the capacitors C_{n-1}, ..., C_1, Co in the array A to the ground of the circuit. On the other hand, by means of the control signal

provided on the output D_{all}, the control module CM causes the closure of the first rail on-off switch S_{Gall} and thereby the connection of the first rail L to the ground of the circuit enforcing in this way a complete discharge of the sampling capacitor C_n and of the capacitors C_{n-1}, ..., C_1, Co in the array A. Afterwards, the control module CM causes, by means of the control signal provided on the output D_n, the closure of the second on-off switch S_{Hn} and thereby the connection of the second rail H to the first rail L and to the ground of the circuit which prevents the occurrence of a random potential on the second rail H. At the same time, the control module CM causes, by means of the control signals provided on the output A_U, the switching of the voltage source change-over switch Su and thereby the connection of the inverting input of the second comparator K2 to the source of the reference voltage U_L. At the same time, the control module CM causes, by means of the control signals provided on the output D_{n-1}, D_{n-2}, ..., D_1, D_0, the opening of the second on-off switches S_{Hn-1}, S_{Hn-2}, ..., S_{H1}, S_{H0}. At the same time, the control module CM causes, by means of the control signal provided on the output A_I, the switching off the current source I, and on the other hand, by means of the control signal provided on the output A_J, the switching off the additional current source J (Fig. 15).

As soon as the control module CM detects the beginning of the active state of the signal on the trigger input InS of the apparatus, the control module CM causes, by means of the control signal provided on the output A_U, the switching of the voltage source change-over switch Su and thereby the connection of the inverting input of the second comparator K2 to the source of the converted voltage U_{IN}. At the same time, the control module CM causes, by means of the control signal provided on the output D_{all}, the opening of the first rail on-off switch S_{Gall} and thereby the disconnection of the first rail L from the ground of the circuit. At the same time, the control module CM causes, by means of the control signals provided on the outputs I_{n-1}, I_{n-2}, ..., I_1, I_0, the opening of the first on-off switches S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} and thereby the disconnection of the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, Co in the array A from the first rail L, and also the switching of the change-over switches S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} and thereby the connection of the bottom plates of the capacitors C_{n-1}, C_{n-2}, ..., C_1, Co to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signal provided on the output A_I, the switching on the current source I (Fig. 16). At the same time, the control module CM deactivates the signal provided on the complete conversion signal output OutR and assigns the initial value zero to all the bits b_{n-1}, b_{n-2}, ..., b_1, bo in the digital word. The electric charge delivered by the use of the current source I is accumulated in the sampling capacitor C_n which is the only capacitor connected at that time to the other end of the current source I through the first rail L and through the closed first on-off switch S_{Ln}. Accumulation of charge in the sampling capacitor C_n causes a progressive increase of the voltage U_n on that capacitor which is compared by the second comparator K2 to the converted voltage U_{IN} value.

When the voltage U_n increasing on the sampling capacitor C_n reaches the converted voltage U_{IN} value which represents the mapping of the converted voltage U_{IN} value to the portion of electric charge proportional to this value and accumulated in the sampling capacitor C_n, the control module CM on the basis of the output signal of the second comparator K2 causes, by means of the control signal provided on the output A_I, the switching off the current source I, and also by means of the control signal provided on the output I_n, the opening of the first on-off switch S_{Ln} and thereby the disconnection of the top plate of the sampling capacitor C_n from the first rail L, and also the concurrent switching of the change-over switch S_{Gn} and thereby the connection of the bottom plate of the sampling capacitor C_n to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signals provided on the output A_U, the switching of the voltage source change-over switch Su and thereby the connection of the inverting input of the second comparator K2 to the source of the reference voltage U_L. Next, by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register in the control module CM, the control module CM assigns the function of the source capacitor C_i whose index is defined by the content of the source capacitor C_i index register to the sampling capacitor C_n. At the same time, by writing the value of the index of the capacitor C_{n-1} having the highest capacitance value in the array A to the destination capacitor C_k index register in the control module CM, the control module CM assigns the function of the destination capacitor C_k whose index is defined by the content of the destination capacitor C_k index register to the capacitor C_{n-1}. Then, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of the destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit. Next, the control module CM causes, by means of the control signal provided on the output A_J, the switching on the additional current source J by the use of which the charge accumulated in the source capacitor C_i is transferred through the second rail H and through the first rail L to the destination capacitor C_k (Fig. 17) while the voltage U_i on the source capacitor C_i progressively decreases whereas at the same time the voltage U_k on the destination capacitor C_k progressively increases.

In case when the voltage U_k on the current destination capacitor C_k reaches the reference voltage U_L value during the charge transfer, the control module CM on the basis of the output signal of the second comparator K2 assigns the value one to the relevant bit b_k in the digital word, and the control module CM causes, by means of the control signal provided on the output I_k, the opening of the first on-off switch S_{Lk} and thereby the disconnection of the top plate of the destination capacitor C_k from the first rail L and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the source of auxiliary voltage U_H. Afterwards, by

reduction of the content of the destination capacitor C_k index register by one, the control module CM assigns the function of the destination capacitor C_k to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before. After that the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of a new destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit.

In case when the voltage U_i on the source capacitor C_i reaches the value zero during the charge transfer, the control module CM, on the basis of the output signal of the first comparator K1 causes, by means of the control signal provided on the output D_i, the opening of the second on-off switch S_{Hi} and thereby the disconnection of the top plate of the source capacitor C_i from the second rail H. At the same time, the control module CM causes, by means of the control signal provided on the output I_k, the opening of the first on-off switch S_{Lk} and thereby the disconnection of the top plate of the destination capacitor C_k from the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the source of auxiliary voltage U_H. Next, the control module CM, on the basis of the output signal of the first comparator K1, by writing the current content of the destination capacitor C_k index register to the source capacitor C_i index register, assigns the function of the source capacitor C_i to the capacitor that until now has acted as the destination capacitor C_k, and after that, the control module CM causes, by means of the control signal provided on the output D_i, the closure of the second on-off switch S_{Hi} and thereby the connection of the top plate of a new source capacitor C_i to the second rail H. Afterwards, by reduction of the content of the destination capacitor C_k index register by one, the control module CM assigns the function of the destination capacitor C_k, whose index is defined by the content of the destination capacitor C_k index register in the control module CM, to the subsequent capacitor in the array A, whose capacitance value is twice as lower as the capacitance value of the capacitor, which acted as the destination capacitor directly before. After that, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of the capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the new destination capacitor C_k to the ground of the circuit (Fig. 18).

In both cases the control module CM continues to control the process of charge transfer on the basis of the output signals of both comparators K1 and K2. Each occurrence of the active state on the output of second comparator K2 causes the assignment of the function of the destination capacitor C_k to the subsequent capacitor in the array A whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before. On the other hand, each occurrence of the active state on the output of the first comparator K1 causes the assignment of the function of the source capacitor C_i to the capacitor that until now has acted as the destination capacitor C_k, and at the same time the assignment of the function of the destination capacitor C_k to the subsequent capacitor in the array A, whose capacitance value is twice as lower as the capacitance value of the capacitor which acted as the destination capacitor directly before. The process of charge redistribution is terminated when the capacitor Co having the lowest capacitance value in the array A stops to act as the destination capacitor C_k. Such situation occurs when the active state appears on the output of the first comparator K1, or on the output of the second comparator K2 during charge transfer to the capacitor Co.

When the active state appears on the output of the second comparator K2, the control module CM assigns the value one to the bit b_0. After termination of redistribution of charge delivered by the use of the current source I and accumulated previously in the sampling capacitor C_n and after assigning the corresponding values to the bits b_{n-1}, b_{n-2}, ..., b_1, bo in the output digital word, the control module CM activates the signal provided on the complete conversion signal output OutR and causes introduction of the apparatus into the relaxation phase by switching off the additional current source J, also the switching of the voltage source change-over switch S_U to the position connecting the inverting input of the second comparator K2 to the source of the reference voltage U_L, also the closure of the first on-off switches S_{Ln} and S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0} and thereby the connection of the top plate of the sampling capacitor C_n and the connection of the top plates of all the capacitors C_{n-1}, C_{n-2}, ..., C_1, Co in the array A to the first rail L, and also the concurrent switching of the change-over switches S_{Gn} and S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0} to the positions connecting the bottom plate of the sampling capacitor C_n and the bottom plates of the capacitors C_{n-1}, C_{n-2}, ..., C_1, Co to the ground of the circuit. At the same time, the control module causes the closure of the first rail on-off switch S_{Gall} and thereby the connection of the first rail L to the ground of the circuit, enforcing a complete discharge of the sampling capacitor C_n and of the capacitors C_{n-1}, C_{n-2}, ..., C_1, Co in the array A, and also the opening of the second on-off switches S_{Hn-1}, S_{Hn-2}, ..., S_{H1}, S_{H0} in the array A, and also the closure of the second on-off switch S_{Hn} and thereby the connection of the second rail H to the first rail L and to the ground of the circuit (Fig. 15), which prevents the occurrence of a random potential on the first rail H.

[0030] The operation of the another version of this apparatus variant consists in that as soon as the control module CM detects the beginning of the active state of the signal on the trigger input InS of the apparatus, the control module CM causes, by means of the control signal provided on the output A_U, the switching of the voltage source change-over switch Su and thereby the connection of the inverting input of the second comparator K2 to the source of the converted

voltage U_{IN}. At the same time, the control module CM causes, by means of the control signal provided on the output D_{all}, the opening of the first rail on-off switch S_{Gall} and thereby the disconnection of the first rail L from the ground of the circuit. At the same time, the control module CM causes, by means of the control signals provided on the outputs I_{n-2}, ..., I_1, I_0, the opening of the first on-off switches S_{Ln}-$_2$,..., S_{L1}, S_{L0} and thereby the disconnection of the top plates of all the capacitors C_{n-2}, ..., C_1, Co in the array A from the first rail L and also the switching of the change-over switches S_{Gn-2}, ..., S_{G1}, S_{G0} and thereby the connection of the bottom plates of the capacitors C_{n-2},..., C_1, Co to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signal provided on the output A_I, the switching on the current source I (Fig. 19). At the same time, the control module CM deactivates the signal provided on the complete conversion signal output OutR and assigns the initial value zero to all the bits b_{n-1}, b_{n-2}, ..., b_1, bo in the digital word. The electric charge is accumulated in the capacitor C_{n-1} and at the same time in the sampling capacitor C_n connected in parallel to the capacitor C_{n-1} in the array A of capacitors which are the only capacitors connected at that time to the other end of the current source I through the first rail L and the closed first on-off switches S_{Ln} and S_{Ln-1}. When the voltage U_n increasing on the sampling capacitor C_n reaches the converted voltage U_{IN} value, the control module CM on the basis of the output signal of the second comparator K2 causes, by means of the control signal provided on the output A_I, the switching off the current source I, and on the other hand, by means of the control signal provided on the output I_n, the opening of the first on-off switch S_{Ln} and thereby the disconnection of the top plate of the sampling capacitor C_n from the first rail L, and also the concurrent switching of the change-over switch S_{Gn} and thereby the connection of the bottom plate of the sampling capacitor C_n to the source of auxiliary voltage U_H. At the same time, the control module CM causes, by means of the control signals provided on the output A_U, the switching of the voltage source change-over switch Su and thereby the connection of the inverting input of the second comparator K2 to the source of the reference voltage U_L. Next, by writing the value of the index of the sampling capacitor C_n to the source capacitor C_i index register in the control module CM, the control module CM assigns the function of the source capacitor C_i whose index is defined by the content of the source capacitor C_i index register to the sampling capacitor C_n. At the same time, by writing the value of the index of the capacitor C_{n-1} having the highest capacitance value in the array A to the destination capacitor C_k index register in the control module CM, the control module CM assigns the function of the destination capacitor C_k whose index is defined by the content of the destination capacitor C_k index register to the capacitor C_{n-1}. Then, the control module CM causes, by means of the control signal provided on the output I_k, the closure of the first on-off switch S_{Lk} and thereby the connection of the top plate of the destination capacitor C_k to the first rail L, and also the concurrent switching of the change-over switch S_{Gk} and thereby the connection of the bottom plate of the destination capacitor C_k to the ground of the circuit. Next, the control module CM causes, by means of the control signal provided on the output A_J, the switching on the additional current source J by the use of which the charge is transferred from the source capacitor C_i through the second rail H and through the first rail L to the destination capacitor C_k (Fig. 17). Next, the control module CM starts to control the process of redistribution of accumulated charge that is terminated when the capacitor Co having the lowest capacitance value in the array A stops to act as the destination capacitor C_k. After that the control module CM activates the signal provided on the complete conversion signal output OutR, and causes introducing the apparatus into the relaxation phase again.

Abbreviations

[0031]

A	array of capacitors
CM	control module
K1	first comparator
K2	second comparator
I	current source
J	additional current source
U_L	source of the reference voltage
U_H	source of auxiliary voltage
U_{IN}	source of the converted voltage
U_{DD}	voltage supply
InS	trigger input
In1	first control input of the control module
In2	second control input of the control module
B	digital output of the control module
E	set of control outputs of the control module
OutR	complete conversion signal output
L	first rail

H	second rail
C_{n-1}, C_{n-2}, ..., C_1,	Co capacitors in the array of capacitors
C_n	sampling capacitor
C_i	source capacitor
C_k	destination capacitor
U_{n-1}, U_{n-2}, ..., U_1, U_0	voltages on the capacitors in the array of capacitors
U_n	voltage on the sampling capacitor
U_i	voltage on the source capacitor
U_k	voltage on the destination capacitor
b_{n-1}, b_{n-2}, ..., b_1,	bo bits in the digital word
S_{Ln}	first on-off switch
S_{Hn}	second on-off switch
S_{Gn}	change-over switch
$S_L n_{-1}$, S_{Ln-2}, ..., S_{L1}, S_{L0}	first on-off switches in the array of capacitors
S_{Hn-1}, S_{Hn-2}, ..., S_{H1}, S_{H0}	second on-off switches in the array of capacitors
S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0}	change-over switches in the array of capacitors
S_{Gall}	first rail on-off switch
S_{Un}	voltage source on-off switch
S_{Un-1}	additional voltage source on-off switch
Su	voltage source change-over switch
S_I	current source change-over switch
A_I, A_J, As, A_U	control outputs of the control module
In, I_{n-1}, I_{n-2}, ..., I_1, I_0	control outputs of the control module
D_n, D_{n-1}, D_{n-2}, ..., D_1, Do, D_{Gall}	control outputs of the control module

Claims

1. Method for conversion of an input voltage value to a digital word having a number of bits equal to n, the method being **characterized by**:

• after detecting a beginning of an active state of a signal on a trigger input (InS) by means of a control module (CM), the input voltage value is translated to a portion of electric charge proportional to this voltage value,
• the portion of charge is accumulated in a sampling capacitor (C_n) by connecting the sampling capacitor (C_n) in parallel to a source of the input voltage (U_{IN}) during the active state of the signal on the trigger input (InS), wherein a duration of the active state of the signal on the trigger input (InS) is not shorter than an assumed minimum value,
• after detecting an end of the active state of the signal on the trigger input (InS) by means of the control module (CM), a function of a source capacitor (C_i) having an index is defined by a content of a source capacitor (C_i) index register in the control module (CM) is assigned by means of the control module (CM) to the sampling capacitor (C_n) by writing a value of an index of the sampling capacitor (C_n) to the source capacitor (C_i) index register,
• at the same time a function of a destination capacitor (C_k) having an index is defined by a content of a destination capacitor (C_k) index register in the control module (CM) is assigned by means of the control module (CM) to a capacitor (C_{n-1}) having the highest capacitance value in an array (A) of capacitors by writing the value of the index of the capacitor (C_{n-1}) having the highest capacitance value to the destination capacitor (C_k) index register, while in the array (A) of capacitors a capacitance value of each capacitor (C_{n-1}, C_{n-2}, ..., C_1, C_0) of a given index is twice as high as a capacitance value of the capacitor of the previous index,
• after that, a process of redistribution of the accumulated charge in capacitors in the array (A) is realized during which charge accumulated in the source capacitor (C_i) is transferred to the destination capacitor (C_k) by the use of a current source (I),
• at the same time a voltage (U_k) increasing on the destination capacitor (C_k) is compared to a reference voltage (U_L) value by the use of a second comparator (K2), and also a voltage (U_i) on the source capacitor (C_i) is observed by a first comparator (K1),
• when the voltage (U_i) on the source capacitor (C_i) observed by the first comparator (K1) equals zero during the charge transfer,

- a function of the source capacitor (C_i) is assigned to a current destination capacitor (C_k) by means of

the control module (CM) on the basis of an output signal of the first comparator (K1) by writing a current content of the destination capacitor (C_k) index register in the control module (CM) to the source capacitor (C_i) index register in the control module (CM),

- a function of the destination capacitor (C_k) is assigned to the subsequent capacitor in the array (A) whose capacitance value is twice lower than the capacitance value of the capacitor that operated as the destination capacitor directly before by reducing the content of the destination capacitor (C_k) index register by one,
- charge transfer from a new source capacitor (C_i) to a new destination capacitor (C_k) is continued by the use of the current source (I),

• when the voltage (U_k) on the destination capacitor (C_k) observed by the second comparator (K2) equals the reference voltage (U_L) value during the transfer of charge from the source capacitor (C_i) to the destination capacitor (C_k):

- the function of the destination capacitor (C_k) is assigned by means of the control module (CM) on the basis of an output signal of the second comparator (K2) to the subsequent capacitor in the array (A) whose capacitance value is twice lower than the capacitance value of the capacitor that operated as the destination capacitor directly before by reducing the content of the destination capacitor (C_k) index register by one,
- the charge transfer from the source capacitor (C_i) to a new destination capacitor (C_k) is continued,

• this process is still controlled by means of the control module (CM) on the basis of the output signals of the comparators (K1) and (K2) until:

- the voltage (U_i) on the source capacitor (C_i) observed by the first comparator (K1) equals zero during a period in which the function of the destination capacitor (C_k) is assigned to a capacitor (C_0) having the lowest capacitance value in the array (A) of capacitors,
- or the voltage (U_0) increasing on the capacitor (C_0) and observed at the same time by the second comparator (K2) equals the reference voltage (U_L) value,

• the value one is assigned to bits in the digital word, corresponding to the capacitors in the array (A) of capacitors, on which the voltage equal to the reference voltage (U_L) value has been obtained, and the value zero is assigned to other bits by means of the control module (CM).

2. Method for conversion as claimed in claim 1 **characterized in that** after detecting the beginning of the active state of the signal on the trigger input (InS) by means of the control module (CM), electric charge is accumulated in the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors and at the same time in the sampling capacitor (C_n) connected in parallel to the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors, by connecting at the same time both the sampling capacitor (C_n) and the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors in parallel to the source of the input voltage (U_{IN}) during the active state of the signal on the trigger input (InS), wherein the capacitance value of the sampling capacitor (C_n) is not smaller than the capacitance value of the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors.

3. Apparatus for conversion of an input voltage value (U_{IN}) to a digital word having a number of bits equal to n, the apparatus comprising:

• a control module (CM) comprising a set of control outputs (E) and a digital output (B) for providing the digital word,
• an array (A) of binary weighted capacitors (C_{n-1}, C_{n-2}, ..., C_1, C_0) including a set of switches adapted to be controlled by the control module (CM) through the set of control outputs (E),

the apparatus **characterized in that**:

the set of switches are adapted to establish connections during a charge redistribution process,

the apparatus further comprising:

• a sampling capacitor (C_n) adapted to accumulate a portion of charge proportional to the input voltage value (U_{IN}),
• a first comparator (K1) and a second comparator (K2) adapted to observe voltages on the sampling capacitor and on capacitors in the array (A) of binary weighted capacitors,

• a controllable current source (I) adapted to transfer charge during the charge redistribution process,
• a source of an auxiliary voltage (U_H) and a source of a reference voltage (U_L),
wherein
• the array (A) of binary weighted capacitors are adapted to be used for charge redistribution and comprises an input coupled to a source of the input voltage (U_{IN}), an input coupled to the source of the reference voltage (U_L), an input coupled to the source of the auxiliary voltage (U_H), an input coupled to the controllable current source (I), a set of control inputs adapted to be coupled to the set of control outputs (E) of the control module (CM), a pair of outputs coupled to inputs of the first comparator (K1), another pair of outputs coupled to inputs of the second comparator (K2), a pair of inputs coupled to the sampling capacitor (C_n),
wherein
• the control module (CM) is adapted to control charge redistribution and further comprises a complete conversion signal output (OutR) for indication of end of conversion, a trigger input (InS) adapted to receive an external signal for external conversion triggering, a further control output (A_I) for controlling the controllable current source (I), a first control input (In1) coupled to an output of the first comparator (K1), and a second control input (In2) coupled to an output of the second comparator (K2),

wherein said apparatus is adapted to perform the steps of the method as defined in claim 1.

4. Apparatus as claimed in claim 3 **characterized in that**:

• the array (A) of capacitors comprises a number of n capacitors (C_{n-1}, C_{n-2}, ..., C_1, C_0), and a capacitance value of a capacitor of a given index is twice as high as a capacitance value of the capacitor of the previous index,
• a top plate of the sampling capacitor (C_n) is connected to the source of the input voltage (U_{IN}) through a closed voltage source on-off switch (S_{Un}) of the set of switches and it is also connected through a closed first on-off switch ($_{SLn}$) of the set of switches to a first rail (L) with which top plates of all the capacitors (C_{n-1}, C_{n-2}, ..., C_1, C_0) in the array (A) of capacitors are connected through corresponding open further first on-off switches (S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0}) of the set of switches,
• the top plate of the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors is also connected through a closed second on-off switch (S_{Hn-1}) of the set of switches to a second rail (H) with which the top plate of the sampling capacitor (C_n) is also connected through an open second on-off switch (S_{Hn}) of the set of switches and with which the top plates of the capacitors (C_{n-2}, ..., C_1, C_0) in the array other than the capacitor (Cn-1) having the highest capacitance value in the array (A) of capacitors are connected through corresponding open further second on-off switches of the set of switches (S_{Hn-2}, ..., S_{H1}, S_{H0}),
• the bottom plate of the sampling capacitor (C_n) is connected to the ground of the circuit through a change-over switch of the set of switches (S_{Gn}) whose moving contact is connected to its first stationary contact and another stationary contact of the change-over switch of the set of switches (S_{Gn}) is connected to the source of auxiliary voltage (U_H) and also to a non-inverting input of the first comparator (K1),
• the bottom plates of all the capacitors (C_{n-1}, C_{n-2}, ..., C_1, C_0) in the array (A) are connected to the source of auxiliary voltage (U_H) through corresponding further change-over switches of the set of switches (S_{Gn-1}, S_{Gn-2},..., S_{G1}, S_{G0}) whose moving contacts are respectively connected to their other stationary contacts, and first stationary contacts of the further change-over switches of the set of switches (S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0}) are connected to the ground of the circuit,
• the first rail (L) is connected to the ground of the circuit through an open first rail on-off switch of the set of switches (S_{Gall}) and to a non-inverting input of the second comparator (K2) whose inverting input is connected to the source of the reference voltage (U_L),
• a second rail (H) is connected to an inverting input of the first comparator (K1),
• moreover, the control input of the first on-off switch of the set of switches (S_{Ln}) and the control inputs of the corresponding further first on-off switches of the set of switches (S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0}) in the array (A) and the control input of the change-over switch of the set of switches (S_{Gn}) and the control inputs of the corresponding further change-over switches of the set of switches (S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0}) in the array (A) are coupled together and connected to corresponding control outputs (I_n) and (I_{n-1}, I_{n-2},..., I_1, I_0) of the set of control outputs (E) of the control module (CM),
• a control input of the second on-off switch of the set of switches (S_{Hn}) and control inputs of the corresponding further second on-off switches of the set of switches (S_{Hn-1}, S_{Hn-2}, ..., S_{H1}, S_{H0}) in the array (A) and a control input of the first rail on-off switch of the set of switches (S_{Gall}) are connected to corresponding control outputs (D_n), (D_{n-1}) D_{n-2}, ..., D_1, D_0) and (D_{all}) of the set of control outputs (E) of the control module (CM),
• one end of the current source (I) is connected to the second rail (H), and the other end of the current source (I) is connected to the first rail (L),

• a control input of the voltage source on-off switch of the set of switches (S_{Un}) is connected to another further control output (A_U) of the set of control outputs (E) of the control module (CM).

5. Apparatus as claimed in claim 4 **characterized in that**:

• the sampling capacitor (C_n) is connected in parallel to the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors, wherein the capacitance value of the sampling capacitor (C_n) is not smaller than the capacitance value of the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors,
• at the same time both the sampling capacitor (C_n) and the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors are connected in parallel to the source of the input voltage (U_{IN}) in a way that:

- the top plate of the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors is connected to the source of the input voltage (U_{IN}) through a closed additional voltage source on-off switch of the set of switches (S_{Un-1}),
- the bottom plate of the capacitor having the highest capacitance value in the array (A) of capacitors (C_{n-1}) is connected to the ground of the circuit through the corresponding further change-over switch of the set of switches (S_{Gn-1}) whose moving contact is connected to its first stationary contact, and the other stationary contact of the corresponding further change-over switch of the set of switches (S_{Gn-1}) is connected to the source of auxiliary voltage (U_H),

• the top plate of the capacitor (C_{n-1}) having the highest capacitance value in the array (A) of capacitors is connected also to the first rail (L) through a closed corresponding further first on-off switch of the set of switches (S_{Ln-1}),
• the control input of the voltage source on-off switch of the set of switches (S_{Un}) and the control input of the additional voltage source on-off switch of the set of switches (S_{Un-1}) are coupled together and connected to the another further control output (A_U) of the set of control outputs (E) of the control module (CM).

Patentansprüche

1. Verfahren zur Umwandlung der elektrischen Ausgangsspannung in ein digitales Wort mit einer Anzahl von Bits n, **dadurch gekennzeichnet, dass**

• nach der Detektion des aktiven Zustands des Signals des Steuermoduls (CM) am Auslösungseingang (InS) die Größe der Eingangsspannung mit proportionalem Wert der elektrischen Ladung abgebildet wird,
• die Größe der Ladung im Probe-Kondensator (C_n) durch eine parallele Schaltung des Kondensators (C_n) mit der Quelle der Eingangsspannung (U_{IN}) für die Dauerzeit des aktiven Zustands des Signals am Auslösungseingang (InS) gesammelt wird, wobei die Dauerzeit des aktiven Zustands des Signals am Auslösungseingang (InS) nicht kürzer als der vorgegebene Minimalwert ist,
• nach der Detektion des Endes des aktiven Zustands des Signals am Auslösungseingang (InS) durch das Steuermodul, die Funktion des Quelle-Kondensators (C_i), dessen Index durch den Inhalt des Registers des Indexes des Quelle-Kondensators (C_i) im Steuermodul (CM) ermittelt wird, mit Hilfe des Steuermoduls (CM) im Probe-Kondensator (C_n) durch die Eingabe des Indexwertes des Probe-Kondensators (C_n) im Register des Quelle-Kondensators (C_i) zugeschrieben wird
• in derselben Zeit die Funktion des Ziel-Kondensators (C_k), dessen Index mit dem Inhalt des Registerindexes des Ziel-Kondensators (C_k) des Steuermoduls (CM) bestimmt wird, mit dem Steuermodul (CM) dem Kondensator (C_{n-i}) mit der größten Kapazität in der Kondensatorenmatrix (A) durch die Angabe des Wertes des Indexes des Ziel-Kondensators (C_{n-1}) im Register des Ziel-Kondensators (C_k) zugeschrieben wird, wobei in der Kondensatorenmatrix (A) der Wert der Kapazität von einzelnen Kondensatoren (C_{n-1}, C_{n-2}, ..., C_1, Co) mit dem jeweiligen Index zweimal größer von der Kapazität des Kondensators mit dem früheren Index ist,
• danach wird der Prozess der Verteilung der elektrischen Ladung in der Kondensatoren-Matrix (A), während der die im Quelle-Kondensator (C_i) gesammelte Ladung mit Hilfe der Stromquelle (I) in den Ziel-Kondensator (C_k) übertragen wird, realisiert,
• gleichzeitig mit Hilfe des Komparators (K2) die im Ziel-Kondensator (C_k) steigende Spannung (U_k) mit der Referenz-Spannung (U_L) verglichen und mit dem ersten Komparator (K1) die Spannung (U_i) am Quelle-Kondensator (C_i) kontrolliert wird,
• und wenn die Spannung (U_i) mit dem ersten Quelle-Komparator (K1) am Quelle-Kondensator (C_i) kontrolliert

wird, beträgt sie Null,

- dann wird aufgrund des Ausgangssignals des ersten Komparators (K1) mit Hilfe des Steuermoduls (CM) dem aktuellen Ziel-Kondensator (C_k) die Funktion des Quelle-Kondensators (C_i) zugeschrieben und der aktuelle Inhalt des Indexes des Ziel-Kondensators (C_i) des Steuermoduls (CM) in das Register des Ziel-Kondensators (C_i) des Steuermoduls (CM) eingetragen,
- und die Funktion des Ziel-Kondensators (C_k) dem weiteren Kondensator in der Kondensatorenmatrix (A) mit einer zweimal kleineren Kapazität des Kondensators, der diese Funktion direkt früher hatte, zugeschrieben wird, wobei der Inhalt des Registers des Indexes des Ziel-Kondensators (C_k) um eins vermindert wird
- die Übertragung der Ladung mit Hilfe der Stromquelle (I) aus dem neuen Quelle-Kondensators (C_i) an den neuen Ziel-Kondensator (C_k) fortgesetzt wird,

• und bei der Übertragung der Ladung aus dem Quelle-Kondensator (C_i) an den Ziel-Kondensator (C_k) die mit dem zweiten Komparator (K2) verglichene Spannung (U_k) am Ziel-Kondensator (C_k) gleich der Referenzspannung (U_L) ist,

- und dann auf Grundlage des Ausgangssignals des zweiten Komparators (K2) die Funktion des Ziel-Kondensators (C_k) dem weiteren Kondensator in der Kondensatoren-Matrix (A) mit einer zweimal kleineren Kapazität des Kondensators, der diese Funktion direkt früher hatte, zugeschrieben wird, wobei der Inhalt des Registers des Indexes des Ziel-Kondensators (C_k) um eins vermindert wird
- die Übertragung der Ladung mit Hilfe der Stromquelle (I) aus dem neuen Quelle-Kondensators (C_i) an den neuen Ziel-Kondensator (Ck) fortgesetzt wird,

• wobei dieser Prozess immer noch mit Hilfe des Steuermoduls (CM) auf Grundlage der Ausgangssignale von Komparatoren (K1) und (K2) so lange kontrolliert wird,

- bis die Funktion des Ziel-Kondensators (C_k) der Kondensator (C_0) mit der kleinsten Kapazität in der Kompensatoren-Matrix (A) hat und die mit Hilfe des ersten Komparators (K1) kontrollierte Spannung (Ui) am Quelle-Kondensator (C_i,) null gleicht
- oder die gleichzeitig mit Hilfe des zweiten Komparators (K2) verglichene steigende Spannung (Uo) am Kondensator (Co) der Referenzspannung (U_L) gleicht,

• wobei den Bits des digitalen Wortes, die den Kondensatoren aus der Kondensatorenmatrix (A) zugeordnet sind, und an denen die gleiche Spannung wie die Referenzspannung (U_L) erreicht wurde, mit Hilfe des Steuermoduls (CM) der Wert eins und den anderen Bits der Wert null mit Hilfe des Steuermoduls (CM) zugeschrieben wird.

2. Verfahren zur Umwandlung nach Anspruch 1, **dadurch gekennzeichnet, dass** nach der Detektion des Steuermoduls (CM) am Anfang des aktiven Zustands des Signals am Auslösungseingang (InS) die elektrische Ladung im Kondensator (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix (A) und gleichzeitig im Probe-Kondensator (C_n) der mit dem Kondensator (Cn-1) mit der größten Kapazität in der Kondensatorenmatrix (A), durch gleichzeitige Verbindung des Probe-Kondensators (C_n) und des Kondensators (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix (A) parallel mit der Quelle der Eingangsspannung (U_{IN}) für die Dauerzeit des aktiven Zustands des Signals am Auslösungseingang (InS) gesammelt wird, wobei die Kapazität der Probe-Kondensators (C_n) nicht kleiner als die Kapazität des Kompensators mit dem größten Kapazität (C_{n-1}) in der Kondensatorenmatrix (A) ist.

3. Vorrichtung zur Umwandlung eines Spannungswertes (U_{IN}) in ein digitales Wort mit einer Anzahl von Bits n, beinhaltend:

• Steuermodul (CM) mit Steuerausgängen (E) und dem digitalen Ausgang (B) für digitale Worte,
• Kondensatorenmatrix (A) mit binär gewichteten Kapazitäten (C_{n-i}, C_{n-2}, ..., C_1, C_0) mit einem System von Schaltern, die an die Steuerung mit dem Steuermodul (CM) durch die Steuerausgänge (E) angepasst sind, das genannte System **dadurch gekennzeichnet, dass**
• es einen Satz von Schaltern zur Aufrechterhaltung der Verbindung bei der Verteilung enthält.
Darüber hinaus enthält das System
• den Probe-Kondensator (C_n) angepasst an die Sammlung eines Teils der Ladung proportional zum Wert der elektrischen Eingangsspannung (U_{IN})

• den ersten Komparator (K1) und den zweiten Komparator (K2), die an die Überwachung der Spannungen am Probe-Kondensator und an den Kondensatoren in der Kondensatoren-Matrix (A) mit binär gewichteten Kapazitäten angepasst sind
• überwachte Stromquelle (I), angepasst an die Übertragung der Ladung bei der Verteilung der Ladung
• Hilfsstromquelle (U_H) und Bezugsspannungsquelle (U_L)
in dem System
• ist die Kondensatorenmatrix (A) mit binär gewichteten Kapazitäten an die Verteilung der Ladung angepasst und enthält einen Eingang, der mit der Quelle der Eingangsspannung verbunden ist (U_{IN}), der Eingang ist mit der Quelle der Bezugsspannung (U_L), einen Eingang mit der Quelle der Bezugsspannung (U_H) verbunden, einen Eingang mit der überwachten Stromquelle (I) verbunden, enthält einen Satz der Steuereingänge, die an die Verbindung mit dem Satz der Steuerausgänge (E) des Steuermoduls (CM) angepasst sind, ein Paar der mit den Eingängen des ersten Komparators (K1) verbundenen Eingänge, ein anderes Paar von mit den Eingängen des zweiten Komparators (K2) verbundenen Eingänge, ein Paar der an den Probe-Kondensator (C_n) angeschlossenen Eingänge
in dem System
• ist das Steuermodul (CM) an die Steuerung der Verteilung der Ladung angepasst und enthält einen Ausgang des Signals der Beendigung des Verarbeitungsprozesses (OutR) zur Generation des Signals der Beendigung des Verarbeitungsprozesses, den Eingang des Auslösungssignals (InS) zum Empfang des externen Signals zur Auslösung der internen Verarbeitung, einen weiteren Eingang (A_1) zur Steuerung der überwachten Stromquelle (I), den ersten Steuereingang (In_1), der an den Ausgang des ersten Komparators (K1) angeschlossen ist und den zweiten Steuereingang (In_2), der an den Ausgang des zweiten Komparators (K2) angeschlossen ist, das genannte System ist an die Ausführung der nachfolgenden Phasen der Art und Weise der Umwandlung nach Anspruch 1 angepasst.

4. Vorrichtung nach Anspruch 3 **dadurch gekennzeichnet, dass**

• die Kondensatorenmatrix (A) n Kondensatoren (C_{n-1}, C_{n-2} ... C_1, C_0) enthält und die Kapazität jedes Kondensator mit dem nächsten Index zweimal größer als die Kapazität des direkt vorherigen Kondensators ist
• der obere Umschlag des Probe-Kondensators (C_n) mit einem geschlossenen Eingangsschalter (S_{Un}) des Schaltersatzes mit der Quelle der Eingangsspannung (U_{IN}) und gleichzeitig mit dem geschlossenen ersten Schalter (S_{Ln}) des Schaltersatzes mit der ersten Schiene (L), mit der die oberen Umschläge aller Kondensatoren (C_{n-1}, C_{n-2}, ..., C_1, Co) der Kondensatorenmatrix (A) mit den entsprechenden geöffneten ersten Schaltern (S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0}) des Schaltersatzes verbunden sind, verbunden ist
• der obere Umschlag des Kondensators (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix (A) gleichzeitig mit dem zweiten geschlossenen Schalter (S_{Hn-1}) des Schaltersatzes mit der zweiten Schiene (H), mit der auch mit dem zweiten geöffneten Schalter (S_{Hn}) des Schaltersatzes der obere Umschlag des Probe-Kondensators (C_n) und die oberen Umschläge der Kondensatoren (C_{n-2}, ... , C_1, C_0) der Kondensatorenmatrix (A) anders als der Kondensator (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix mit den geöffneten zweiten Schaltern (S_{Hn-2}, ... , S_{H1}, S_{H0}) verbunden sind, verbunden ist
• der untere Umschlag des Probe-Kondensators (C_n) mit der Masse des Systems mit dem Schalter (S_{Gn}) des Schaltersatzes, dessen Arbeitskontakt mit seinem ersten Ruhekontakt geschlossen ist, verbunden ist und der zweite Ruhekontakt dieses Schalters (S_{Gn}) des Schaltersatzes mit der Quelle der Hilfsspannung (U_H) und gleichzeitig mit dem nichtinvertierenden Eingang des ersten Komparators (K1) verbunden ist
• die unteren Umschläge aller Kondensatoren (C_{n-1}, C_{n-2}, ..., C_1, Co) der Kondensatorenmatrix (A) mit der Quelle der Hilfsspannung (U_H) mit nachfolgenden Schaltern (S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0}), deren Arbeitskontakte mit denen zweiten Ruhekontakten geschlossen sind, verbunden sind, und die ersten Ruhekontakte dieser Schalter (S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0}) mit der Masse des Systems verbunden sind
• die erste Schiene (L) mit der Masse des Systems mit dem ersten geöffneten Schalter der Schiene (S_{Gall}) und dem nichtinvertierenden Eingang des zweiten Komparators (K2) verbunden ist und der invertierende Eingang dieses Komparators mit der Quelle der Bezugsspannung (U_L) verbunden ist
• die zweite Schiene (H) mit dem invertierenden Eingang des erstens Komparators (K1) verbunden ist
• und darüber hinaus die Steuereingänge des ersten Schalters (S_{Ln}) des Schaltersatzes und die Steuereingänge der Schalter (S_{Ln-1}, S_{Ln-2} .... ,S_{L1}, S_{L0}) der Kondensatorenmatrix (A) sowie der entsprechenden Steuereingang des Schalters (S_{Gn}) und die Steuereingänge der Schalter (S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0}) in der Kondensatorenmatrix miteinander gekoppelt und mit den entsprechenden Steuerausgängen (In) und (I_{n-1}, I_{n-2}, ..., I_1,I_0) den Steuerausgängen (E) des Steuermoduls (CM) verbunden sind
• die Steuereingänge des zweiten Schalters (S_{Hn}) des Schaltersatzes und die Steuereingänge der nachfolgenden Schalter (S_{Hn-1}, S_{Hn-2}, $S_{H1,}$ S_{H0}) der Kondensatorenmatrix (A) sowie der Steuereingang (S_{Gall}) des ersten

Schalters der Schiene im Schaltersatz mit entsprechenden Steuerausgänge (D_n),(D_{n-1}, D_{n-2}, ..., D_1, Do) (D_{all}) des Satzes der Steuerausgänge (E) des Moduls (CM) verbunden sind
• ein Pol der Stromquelle (I) mit der zweiten Schiene (H) und ihr zweiter Pol mit der ersten Schiene (L) verbunden ist
• der Steuereingang des Schalters der Stromquelle (S_{Un}) des Schaltersatzes mit dem Steuerausgang (Au) des Satzes der Steuerausgänge (E) des Moduls (CM) verbunden ist.

5. Vorrichtung nach Anspruch 4 **dadurch gekennzeichnet, dass**

• der Probe-Kondensator (C_n) parallel mit dem Kondensator (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix (A) verbunden ist, wobei die Kapazität des Probe-Kondensators (C_n) nicht kleiner als die Kapazität des Kondensators (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix (A) ist
• der Probe-Kondensator (C_n) und gleichzeitig der Kondensator (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix (A) parallel mit der Quelle der Eingangsspannung (U_{IN}) so verbunden sind, dass:

- der obere Umschlag des Kondensators (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix (A) mit der Quelle der Eingangsspannung (U_{IN}) mit geschlossenem Eingangsschalter (S_{Un-1}) des Schaltersatzes verbunden ist
- der untere Umschlag des Kondensators (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix (A) mit der Masse des Systems mit dem entsprechenden Schalter (S_{Gn-1}) des Schaltersatzes verbunden ist sowie der Arbeitskontakt mit dem ersten Ruhekontakt geschlossen ist und der zweite Ruhekontakt dieses Schalters (S_{Gn-1}) des Schaltersatzes mit der Quelle der Hilfsspannung (U_H) verbunden ist,

• der Probe-Kondasator (
• der obere Umschlag des Kondensators (C_{n-1}) mit der größten Kapazität in der Kondensatorenmatrix (A) auch mit der ersten Schiene (L) mit dem entsprechenden geschlossenen ersten Schalter (S_{Ln-1}) des Schaltersatzes verbunden ist
• der Steuereingang des Eingangsschalters (S_{Un}) des Schaltersatzes und der Steuereingang des Eingangsschalters (S_{Un-1}) des Schaltersatzes miteinander und gemeinsam mit dem nächsten Steuerausgang (A_U) des Satzes der Steuerausgänge (E) des Steuermoduls (CM) verbunden sind.

Revendications

1. Procédé permettant de convertir une valeur de tension en mot numérique d'un nombre de bits égal à n, **caractérisé en ce que**

• après la détection au moyen du module de commande (CM) du début de l'état actif du signal sur l'entrée de déclenchement (InS), la valeur de la tension d'entrée se mappe par la valeur proportionnelle de la charge électrique,
• la charge s'accumule dans le condensateur d'échantillonnage (C_n) par l'association en parallèle du condensateur (C_n) avec la source de tension d'entrée (U_{IN}) pour la durée de l'état actif du signal sur l'entrée de déclenchement (InS), étant précisé que la durée de l'état actif du signal sur l'entrée de déclenchement (InS) n'est pas inférieure à la valeur minimale fixée,
• après la détection au moyen du module de commande (CM) de la fin de l'état actif du signal sur l'entrée de déclenchement (InS), la fonction de condensateur de source (C_i), dont l'indice est défini par le contenu du registre de l'indice du condensateur de source (C_i) dans le module de commande (CM) est attribuée au moyen du module de commande (CM) au condensateur d'échantillonnage (C_n), par l'inscription de la valeur de l'indice du condensateur d'échantillonnage (C_n) au registre de l'indice du condensateur de source (C_i),
• dans le même temps, la fonction de condensateur de destination (C_k), dont l'indice est défini par le contenu du registre de l'indice du condensateur de destination (C_k) du module de commande (CM), est attribuée au moyen du module de commande (CM) au condensateur (C_{n-i}) ayant la capacité la plus élevée dans le réseau de condensateurs (A) par l'inscription au registre de l'indice du condensateur de destination (C_k) de la valeur de l'indice du condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A), étant précisé que, dans le réseau de condensateurs (A) la valeur de la capacité de chacun des condensateurs (C_{n-1}, C_{n-2}, ..., C_1, Co) ayant un indice donné est deux fois plus élevée que la capacité du condensateur ayant l'indice précédent,
• ensuite est réalisé le processus de redistribution de la charge électrique stockée dans le réseau de conden-

sateurs (A), lors duquel la charge stockée dans le condensateur de source (C_i) est transférée au moyen de la source de courant (I) au condensateur de destination (C_k)

• en même temps, au moyen du comparateur (K2) est comparée la tension (U_k) croissante sur le condensateur de destination (C_k) avec la tension de référence (U_L) et est contrôlée, au moyen du premier comparateur (K1), la tension (U_i) sur le condensateur de source (C_i),

• et lorsque la tension (U_i) contrôlée au moyen du premier comparateur (K1) sur le condensateur de source (C_i) est égale à zéro,

■ alors, sur la base du signal de sortie du premier comparateur (K1) au moyen du module de commande (CM) à l'actuel condensateur de destination (C_k) est attribuée la fonction de condensateur de source (C_i) par l'inscription au registre de l'indice du condensateur de source (C_i) du module de commande (CM) de la valeur actuelle du registre de l'indice du condensateur de destination (C_k) du module de commande (CM),

■ et la fonction de condensateur de destination (C_k) est attribuée au condensateur suivant du réseau de condensateurs (A) d'une capacité deux fois plus petite que la capacité du condensateur qui a rempli cette fonction directement précédemment, en diminuant de « un » le contenu du registre de l'indice condensateur de destination (C_k),

■ est poursuivi le transfert de la charge au moyen de la source de courant (I) du nouveau condensateur de source (C_i) au nouveau condensateur de destination (C_k),

• et lorsque, lors du transfert de la charge du condensateur de source (C_i) au condensateur de destination (C_k), la tension (U_k) sur le condensateur de destination (C_k), comparée au moyen du second comparateur (K2), égale à la tension de référence (U_L),

▪ alors, sur la base du signal de sortie du second comparateur (K2), au moyen du module de commande (CM), la fonction de condensateur de destination (C_k) est attribuée au condensateur suivant du réseau de condensateurs (A) d'une capacité deux fois plus petite que la capacité du condensateur qui a rempli cette fonction directement précédemment en diminuant de « un » le contenu du registre de l'indice du condensateur de destination (C_k),

▪ est poursuivi le transfert de la charge du condensateur de source (C_i) au nouveau condensateur de destination (Ck),

• étant précisé que ce processus est toujours contrôlé au moyen du module de commande (CM) sur la base des signaux de sortie des comparateurs (K1) et (K2) jusqu'au moment

▪ où, lors de l'exercice de fonction de condensateur de destination (C_k) par le condensateur (Co) ayant la capacité la plus petite dans le réseau de condensateurs (A), la tension (U_i) sur le condensateur source (C_i,) contrôlée au moyen du premier comparateur (K1), est égale à zéro ,

▪ ou, la tension (Uo) croissante sur le condensateur (Co), comparée dans le même temps au moyen du second comparateur (K2), est égale à la tension de référence (U_L),

• étant précisé qu'aux bits du mot numérique correspondant aux condensateurs du réseau de condensateurs (A), pour lesquels a été obtenue la tension ayant la valeur de la tension de référence (U_L), est attribuée au moyen du module de commande (CM) la valeur « une » et aux autres bits est attribuée au moyen du module de commande (CM) la valeur zéro.

2. Le procédé de conversion selon la revendication 1, **caractérisé en ce que** après la détection au moyen du module de commande (CM) du début de l'état actif du signal sur l'entrée de déclenchement (InS) la charge électrique s'accumule dans le condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A) et, en même temps, dans le condensateur d'échantillonnage (C_n) associé en parallèle avec le condensateur (Cn-1) ayant la capacité la plus élevée dans le réseau de condensateurs (A), par l'association simultanée aussi bien du condensateur d'échantillonnage (C_n) que du condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A) en parallèle avec la source de tension d'entrée (U_{IN}) pour la durée de l'état actif du signal sur l'entrée de déclenchement (InS), étant précisé que la capacité du condensateur d'échantillonnage (C_n) n'est pas inférieure à la capacité du condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A).

3. Appareil pour conversion de valeur de tension d'entrée (U_{IN}) en mot numérique ayant le nombre de bits n, comprenant :

• un module de commande (CM) comprenant un ensemble de sorties de commande (E) et une sortie numérique (B) pour mots numériques,
• un réseau de condensateurs (A) à graduations binaires (C_{n-i}, C_{n-2}, ..., C_1, Co) comprenant un ensemble de commutateurs adaptés à la commande au moyen du module de commande (CM) par un ensemble de sorties de commande (E)
l'appareil susvisé **caractérisé en ce que**
• il comprend un ensemble de commutateurs adapté pour maintenir la connexion lors du processus de redistribution
en outre, l'appareil comprend
• un condensateur d'échantillonnage (C_n) adapté au stockage de la charge proportionnelle à la valeur de la tension du courant d'entrée (U_{IN}),
• le premier comparateur (K1) et le second comparateur (K2) adaptés pour contrôler les tensions sur le condensateur d'échantillonnage et sur les condensateurs du réseau de condensateurs (A) à graduations binaires,
• une source de courant contrôlable (I) adaptée pour transférer la charge lors du processus de redistribution de la charge,
• une source de tension auxiliaire (U_H) et une source de tension de référence (U_L),
où, dans ledit appareil
• le réseau de condensateurs (A) à graduations binaires est adapté à la redistribution de la charge et comprend une entrée connectée à la source de tension d'entrée (U_{IN}), ladite entrée est connectée à la source de tension de référence (U_L), une entrée connectée à la source de tension auxiliaire (U_H), une entrée connectée à la source de courant contrôlable (I), un ensemble d'entrées de commande adaptées pour être connectées à l'ensemble de sorties de commande (E) du module de commande (CM), une paire de sorties connectées aux entrées du premier comparateur (K1), une autre paire de sorties connectées aux entrées du second comparateur (K2), une paire d'entrées connectées au condensateur d'échantillonnage (C_n)
où, dans ledit appareil
• le module de commande (CM) est adapté à la commande de la redistribution de la charge et comprend, de plus, une sortie du signal de fin de processus de conversion (OutR) pour la génération du signal de fin de processus de conversion, une entrée du signal de déclenchement (InS) pour recevoir le signal externe pour déclencher la conversion interne, une sortie suivante (A_1) pour commander la source de courant contrôlable (I), une première l'entrée de commande (In_1) connectée à la sortie du premier comparateur (K1) et une seconde entrée de commande (In_2) connectée à la sortie du second comparateur (K2)
l'appareil susvisé est adapté pour exécuter les étapes successives du procédé selon la revendication 1.

4. L'appareil selon la revendication 3 **caractérisé en ce que**

• le réseau de condensateurs (A) comprend n condensateurs (C_{n-1}, C_{n-2} ... C_1, Co), et la capacité de chacun des condensateurs d'un indice successif est deux fois plus élevée que la capacité du condensateur qui le précède directement,
• l'armature supérieure du condensateur d'échantillonnage (C_n), est connectée par un coupleur d'entrée fermé (S_{Un}) de l'ensemble de coupleurs à la source de tension d'entrée (U_{IN}) et, dans le même temps, par le premier coupleur fermé (S_{Ln}) de l'ensemble de coupleurs avec le premier rail (L), auquel sont connectées les armatures supérieures de tous les condensateurs (C_{n-1}, C_{n-2}, ..., C_1, Co) du réseau de condensateurs (A) par les premiers coupleurs appropriés ouverts (S_{Ln-1}, S_{Ln-2}, ..., S_{L1}, S_{L0}) de l'ensemble de coupleurs,
• l'armature supérieure du condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A) est, dans le même temps, connectée par le second coupleur fermé (S_{Hn-1}) de l'ensemble de coupleurs au second rail (H), auquel est aussi connectée, par le second coupleur ouvert (S_{Hn}) de l'ensemble de coupleurs, l'armature supérieure du condensateur d'échantillonnage (C_n) et les armatures supérieures des condensateurs (C_{n-2}, ... , C_1, Co) du réseau de condensateurs (A) autres que le condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs par les seconds coupleurs ouverts (S_{Hn-2}, ... , S_{H1}, S_{H0}),
• l'armature inférieure du condensateur d'échantillonnage (C_n) est connectée à la masse de l'appareil par le commutateur (S_{Gn}) de l'ensemble de coupleurs, dont la borne mobile est connectée à sa première borne fixe, et la seconde borne fixe de ce commutateur (S_{Gn}) de l'ensemble de coupleurs est connectée à la source de tension auxiliaire (U_H) et, dans le même temps, à l'entrée non inverseuse du premier comparateur (K1),
• les armatures inférieures de tous les condensateurs (C_{n-1}, C_{n-2}, ..., C_1, Co) dans le réseau de condensateurs (A) sont connectées à la source de tension auxiliaire (U_H) par les commutateurs successives (S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0}), dont les bornes mobiles sont de manière appropriée connectées à leurs secondes bornes fixes et les premières bornes fixes de ces commutateurs (S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0}) sont connectées à la masse de l'appareil,

• le premier rail (L) est connecté à la masse de l'appareil par le premier commutateur ouvert du rail (S_{Gall}) et avec l'entrée non inverseuse du second comparateur (K2), dont entrée inverseuse est connectée à la source de tension de référence (U_L),
• le second rail (H) est connecté à l'entrée inverseuse du premier comparateur (K1),
• de plus, les entrées de commande du premier commutateur (S_{Ln}) de l'ensemble de coupleurs et les entrées de commande des commutateurs successives (S_{Ln-1}, S_{Ln-2} .... ,S_{L1}, S_{L0}) dans le réseau de condensateurs (A) et l'entrée correspondant de commande du commutateur (S_{Gn}) et les entrées de commande des commutateurs successives (S_{Gn-1}, S_{Gn-2}, ..., S_{G1}, S_{G0}) dans le réseau de condensateurs (A) sont accouplées et sont connectées aux sorties de commande correspondantes (I_n) et (I_{n-1}, I_{n-2}, ..., I_1,I_0) des sorties de commande (E) du module de commande (CM),
• les entrées de commande du second commutateur (S_{Hn}) de l'ensemble de coupleurs et les entrées de commande des commutateurs successives (S_{Hn-1}, S_{Hn-2}, S_{H1}, S_{H0}) du réseau de condensateurs (A) et l'entrée de commande (S_{Gall}) du premier commutateur du rail dans l'ensemble de coupleurs sont connectées aux sorties de commande (D_n),(D_{n-1}, D_{n-2}, ..., D_1, D_0) (D_{all}) correspondantes de l'ensemble de sorties de commande (E) du module (CM)
• l'un des pôles de la source de courant (I) est connecté au second rail (H), et son second pôle est connecté au premier rail (L),
• l'entrée de commande du commutateur de la source de courant (S_{Un}) de l'ensemble de commutateurs est connectée à la sortie de commande (A_U) de l'ensemble de sorties de commande (E) du module (CM).

5. L'appareil selon la revendication 4 **caractérisé en ce que**

• le condensateur d'échantillonnage (C_n) est associé en parallèle avec le condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A) où la capacité condensateur d'échantillonnage (C_n) n'est pas plus petite que la capacité du condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A)
• en même temps, le condensateur d'échantillonnage (C_n) et le condensateur(C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A) sont associés en parallèle avec la source de tension d'entrée (U_{IN}), de sorte que :

- l'armature supérieure du condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A) est connectée à la source de tension d'entrée (U_{IN}) par le coupleur d'entrée relié (S_{Un-1}) de l'ensemble de coupleurs,
- l'armature inférieure du condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A) est connectée à la masse de l'appareil par le commutateur (S_{Gn-1}) lui correspondant de l'ensemble de coupleurs, dont la borne mobile est reliée à la première borne fixe et la seconde borne fixe de ce commutateur (S_{Gn-1}) de l'ensemble de coupleurs est connectée à la source de tension auxiliaire (U_H),

• l'armature supérieure du condensateur (C_{n-1}) ayant la capacité la plus élevée dans le réseau de condensateurs (A) est connectée aussi au premier rail (L) par le premier coupleur (S_{Ln-1}) relié lui correspondant de l'ensemble de coupleurs,
• l'entrée de commande du coupleur d'entrée (S_{Un}) de l'ensemble de commutateurs et l'entrée de commande du coupleur d'entrée (S_{Un-1}) de l'ensemble de commutateurs sont connectées entre elles et, ensemble, connectées à la sortie de commande (A_U) successive de l'ensemble de sorties de commande (E) du module de commande (CM).

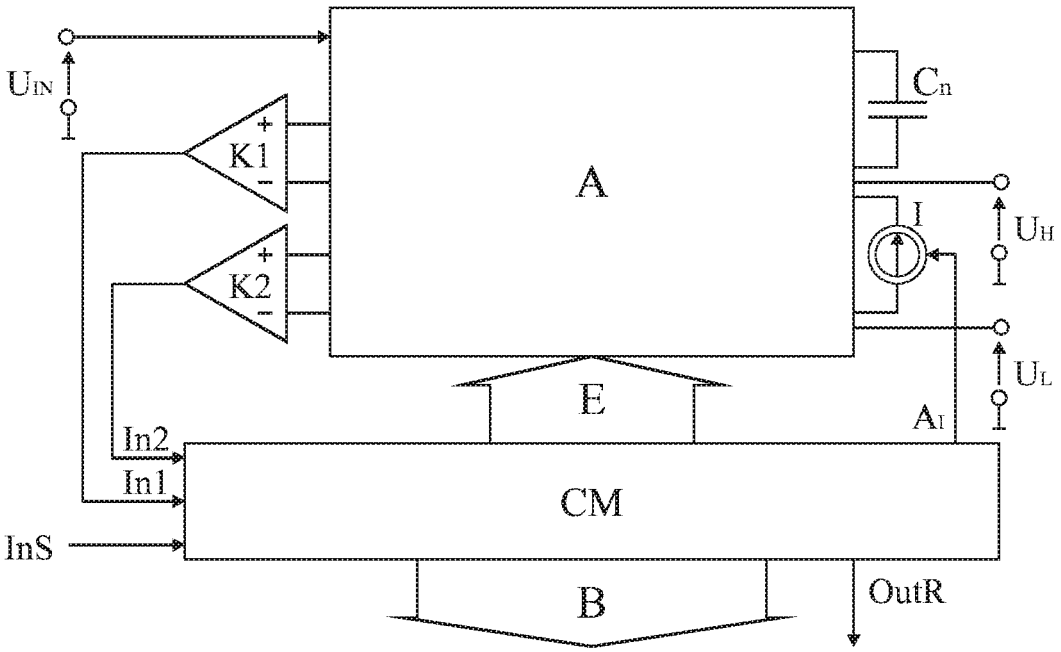

Fig. 1

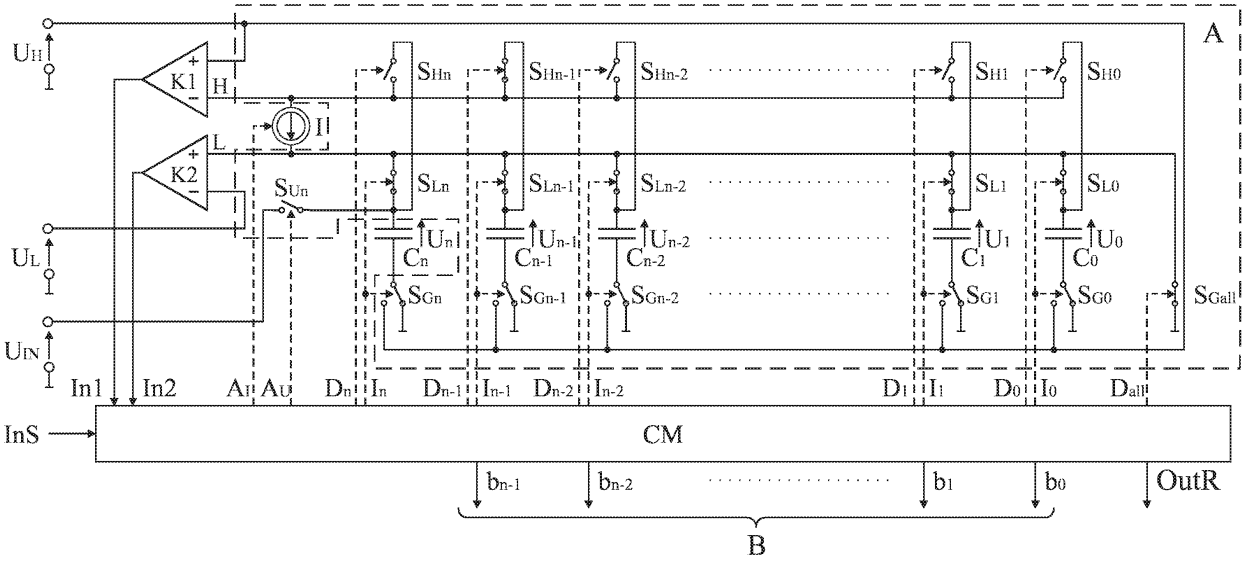
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Fig. 2

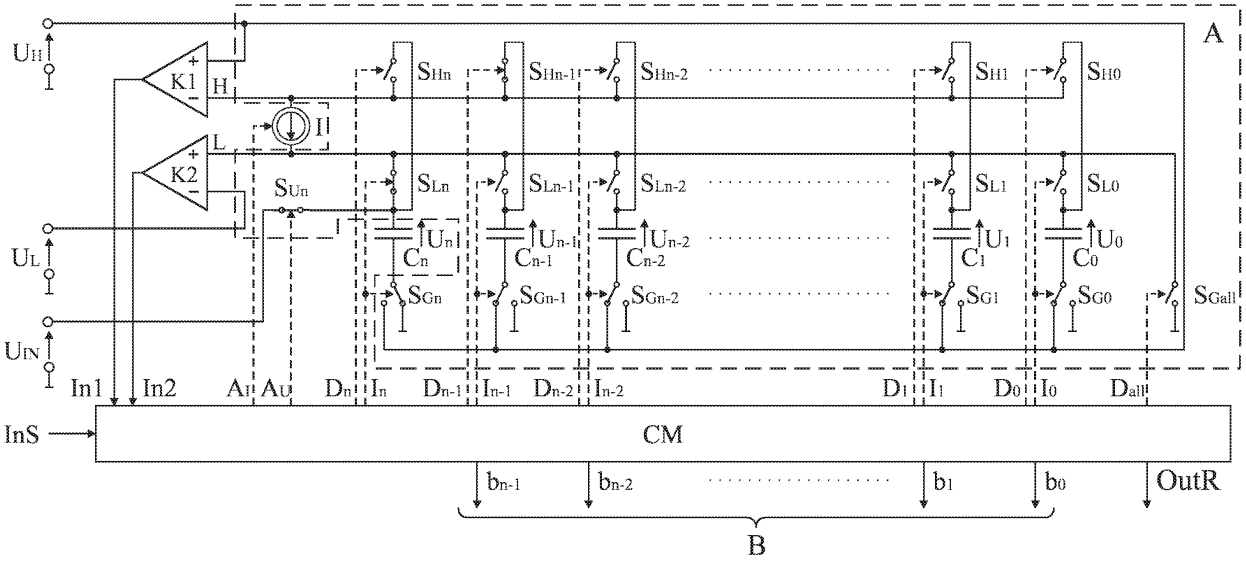
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Fig. 3

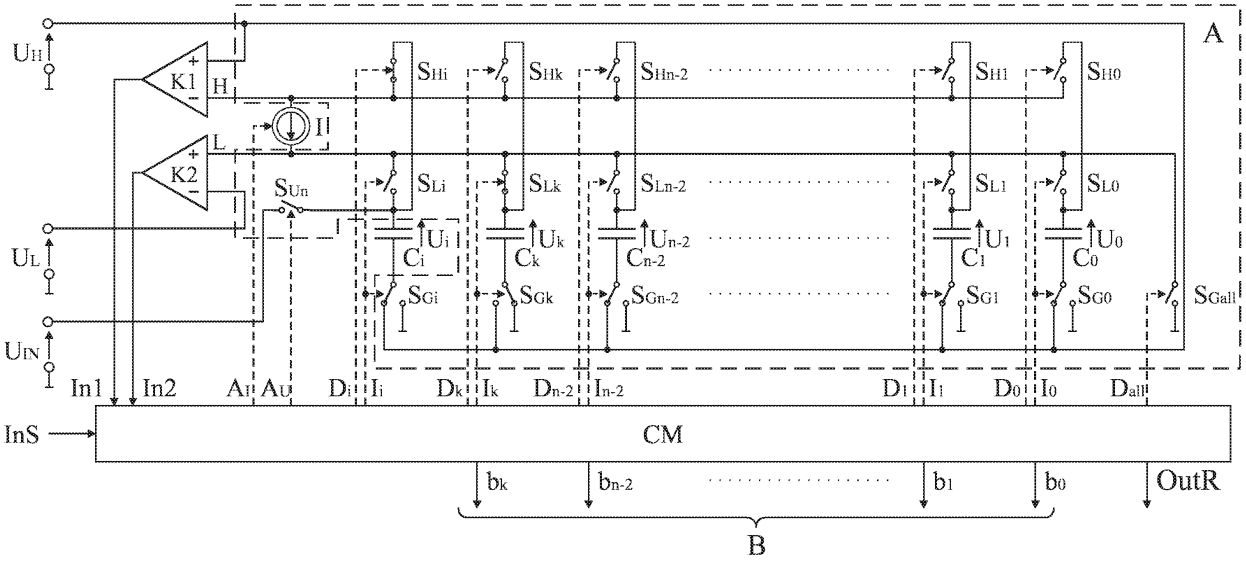
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Fig. 4

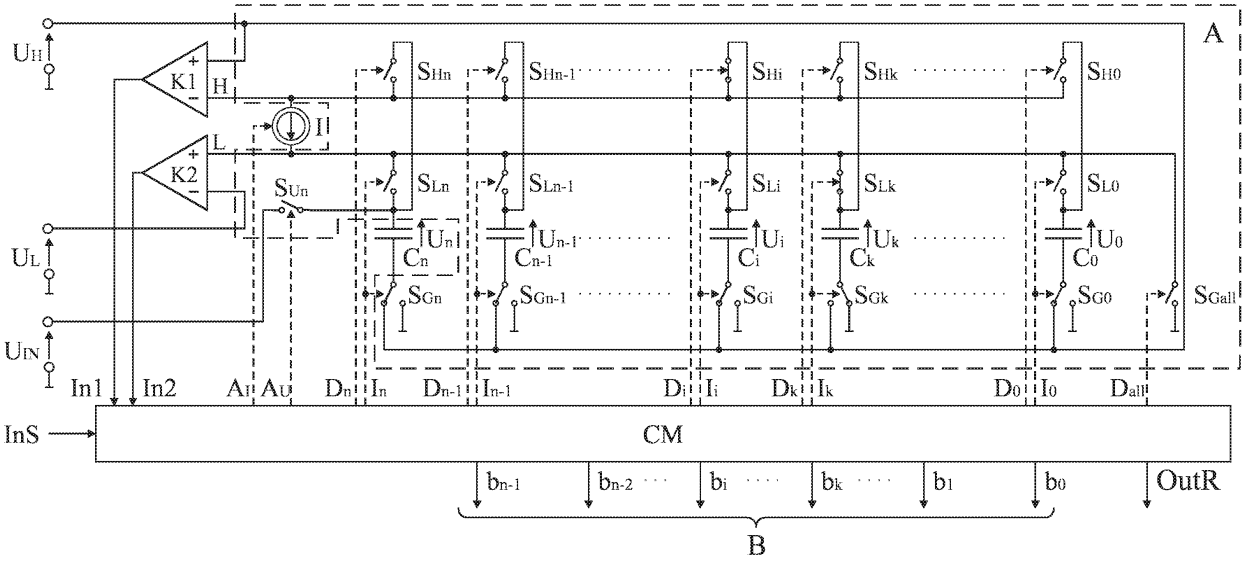
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Fig. 5

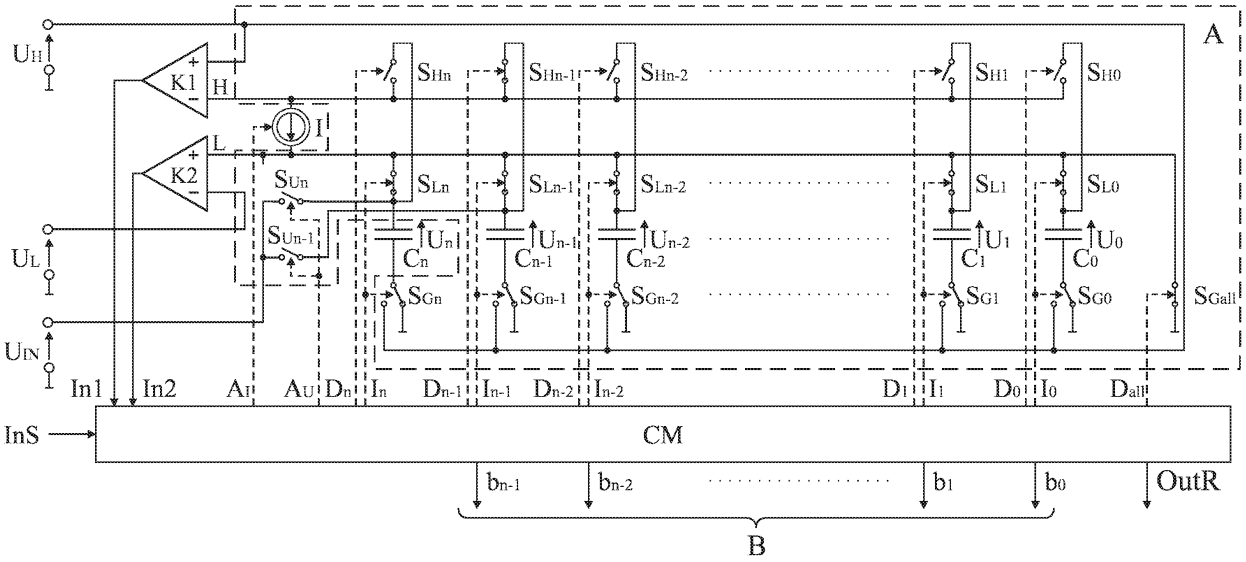
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Fig. 6

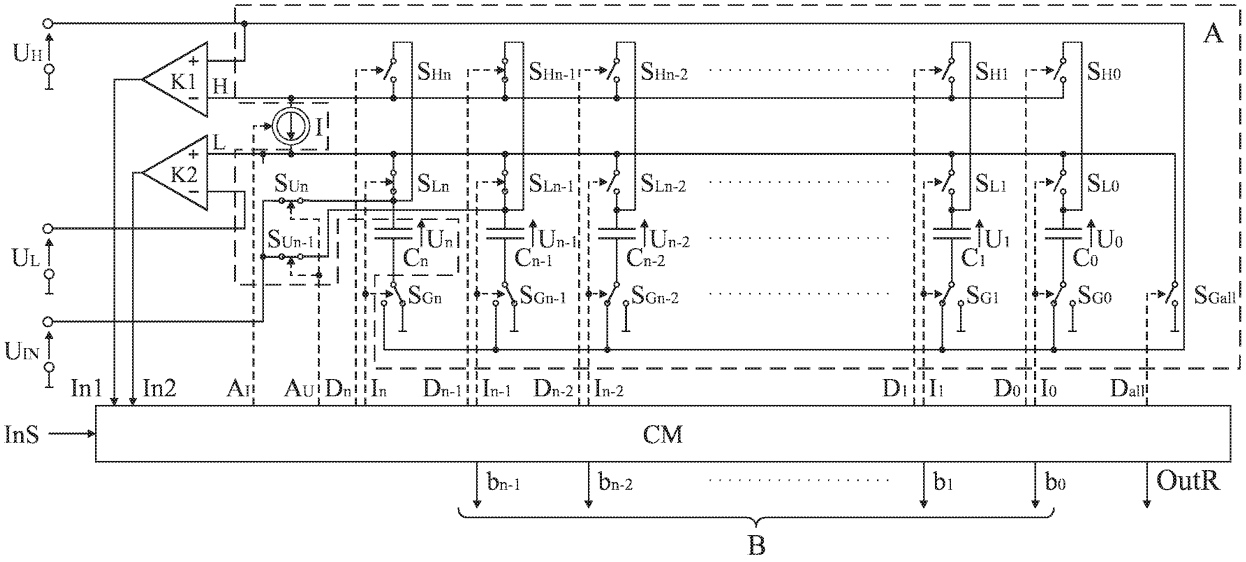
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Fig. 7

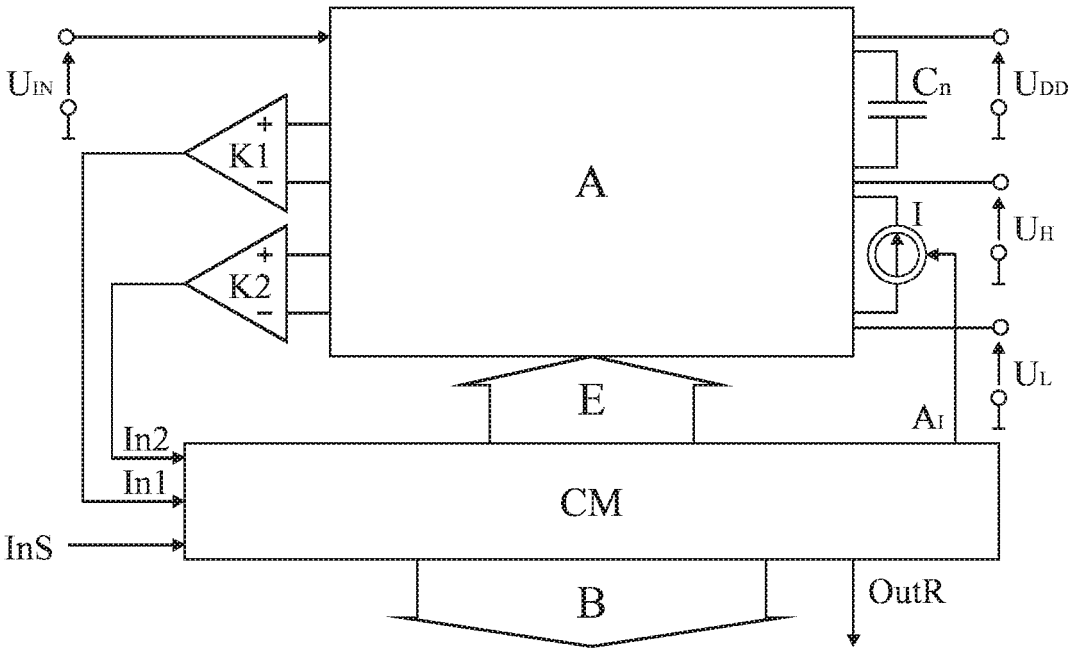

Fig. 8

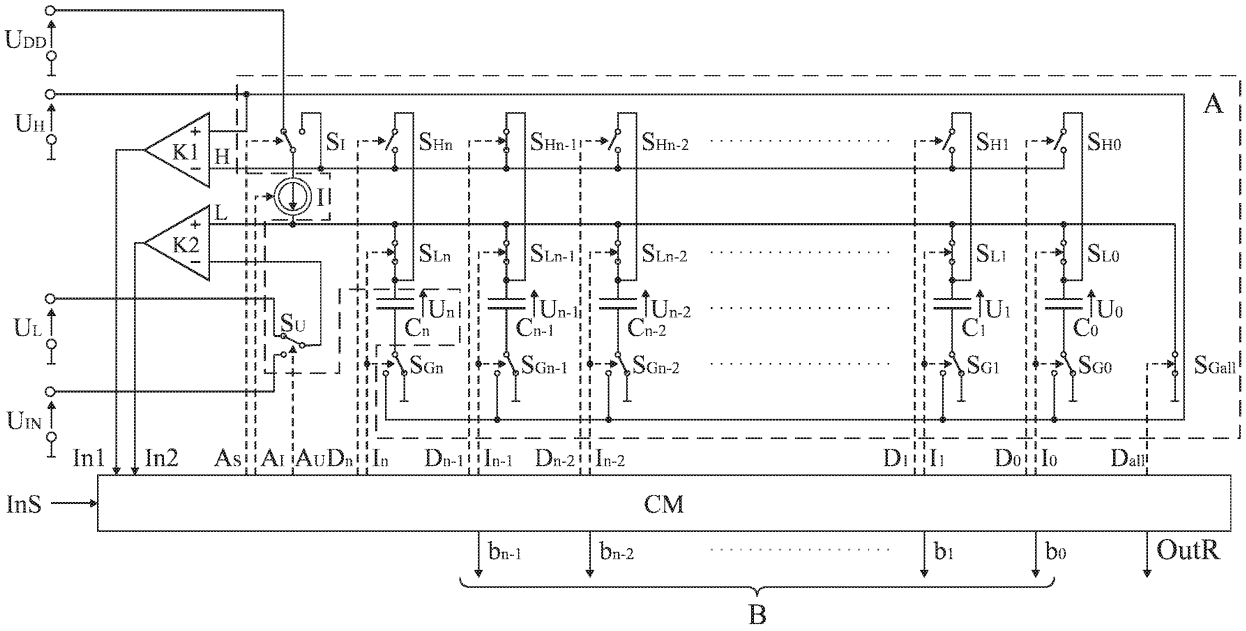
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Fig. 9

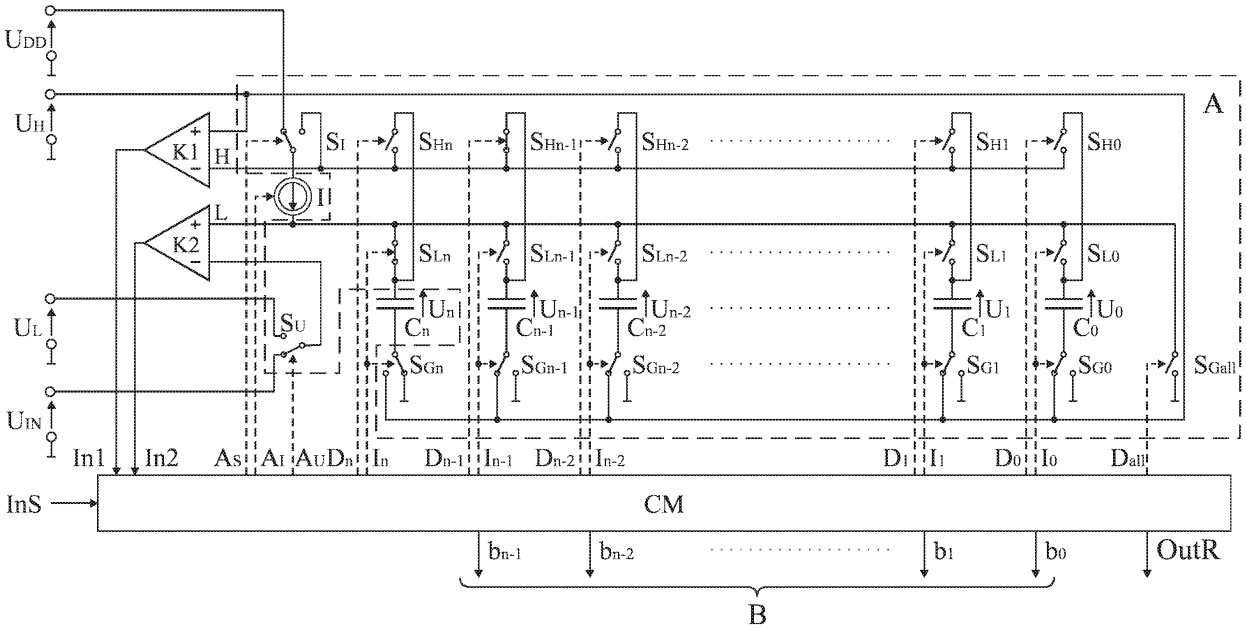
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Fig. 10

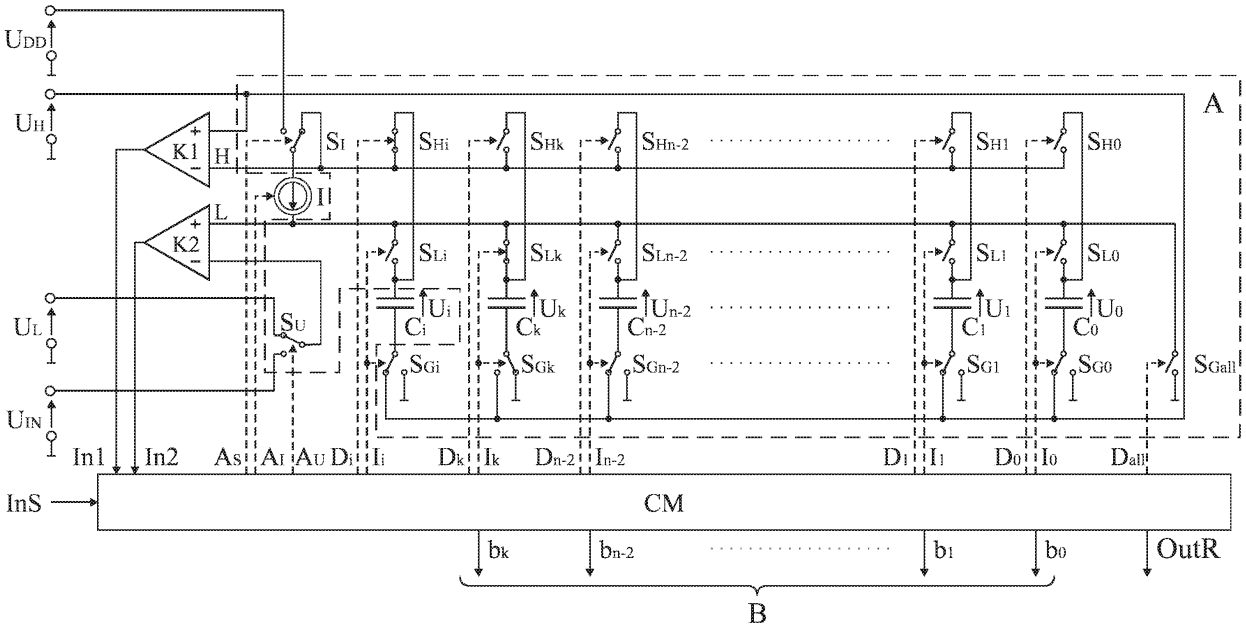
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Fig. 11

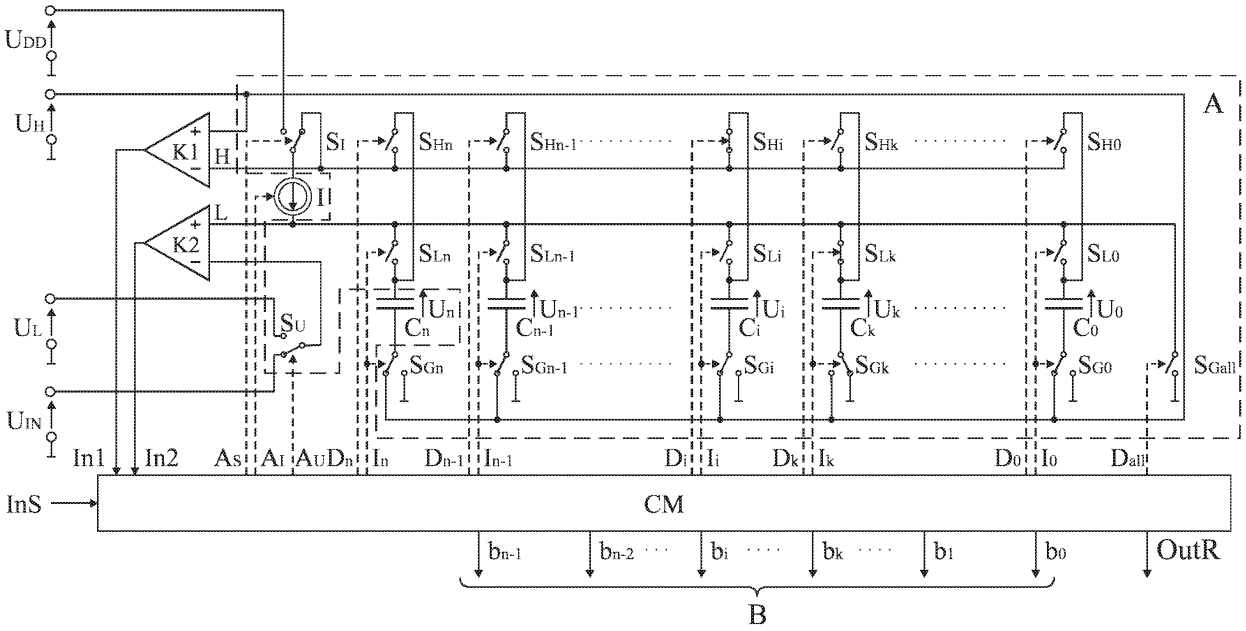
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Fig. 12

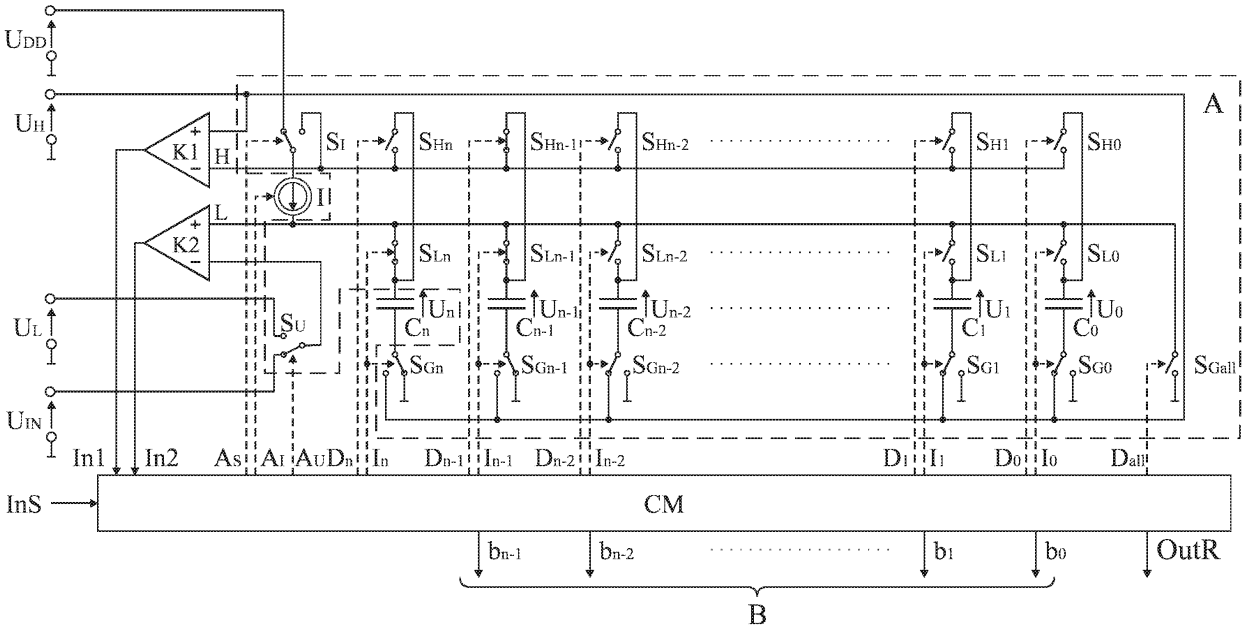
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Fig. 13

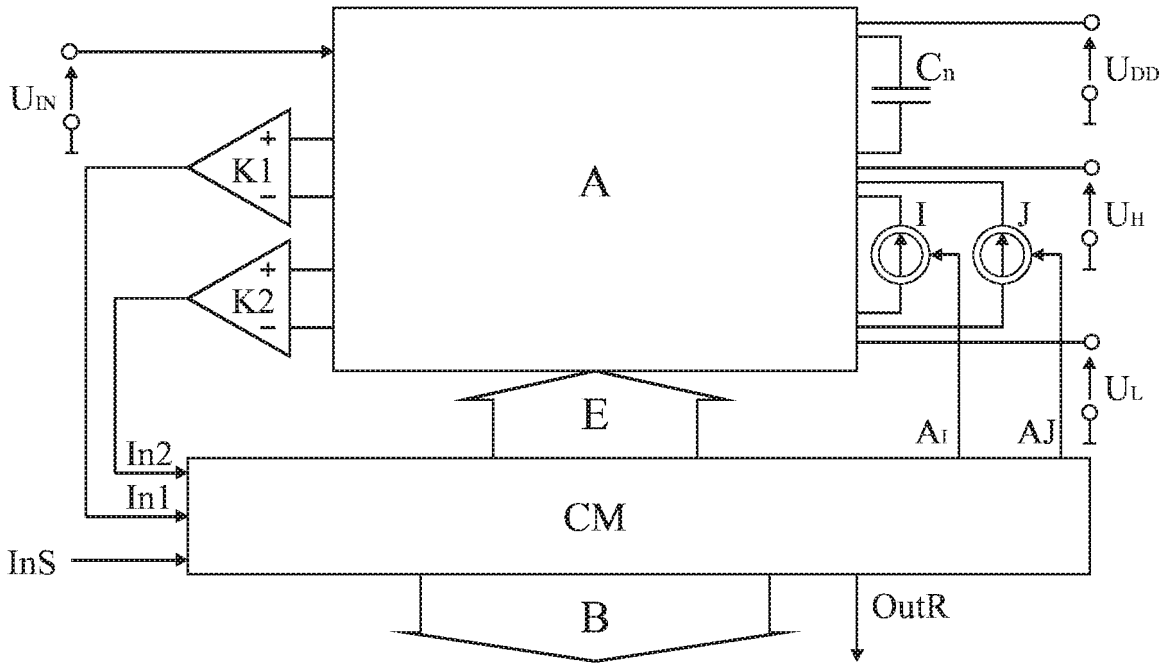

Fig. 14

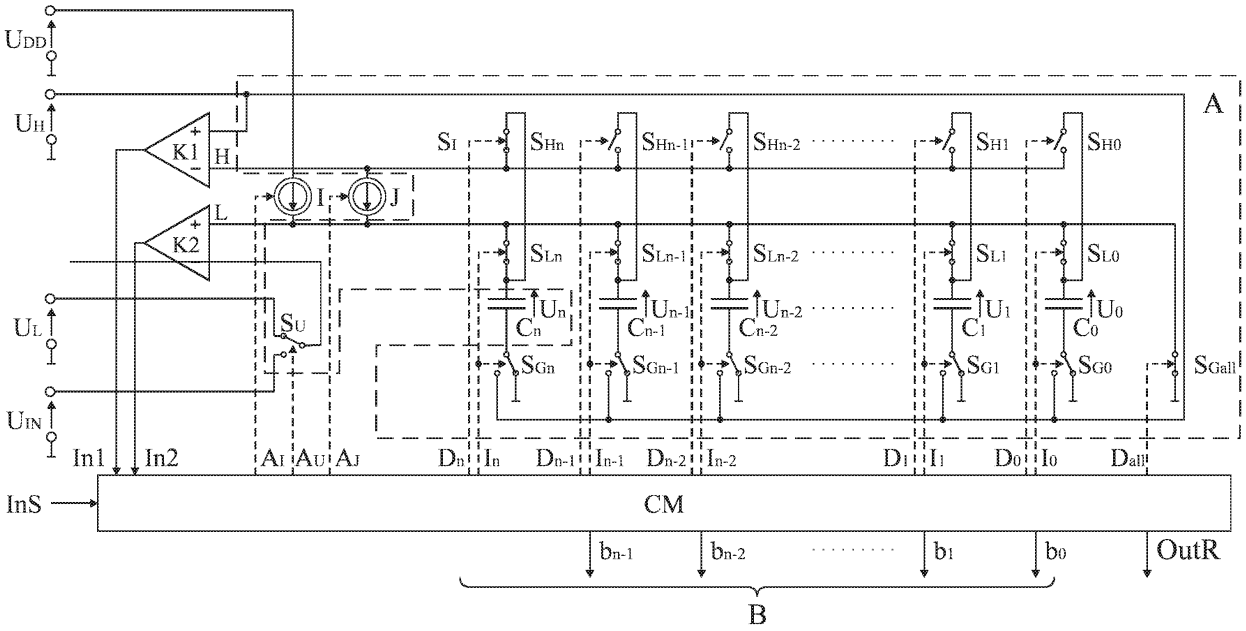
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Fig. 15

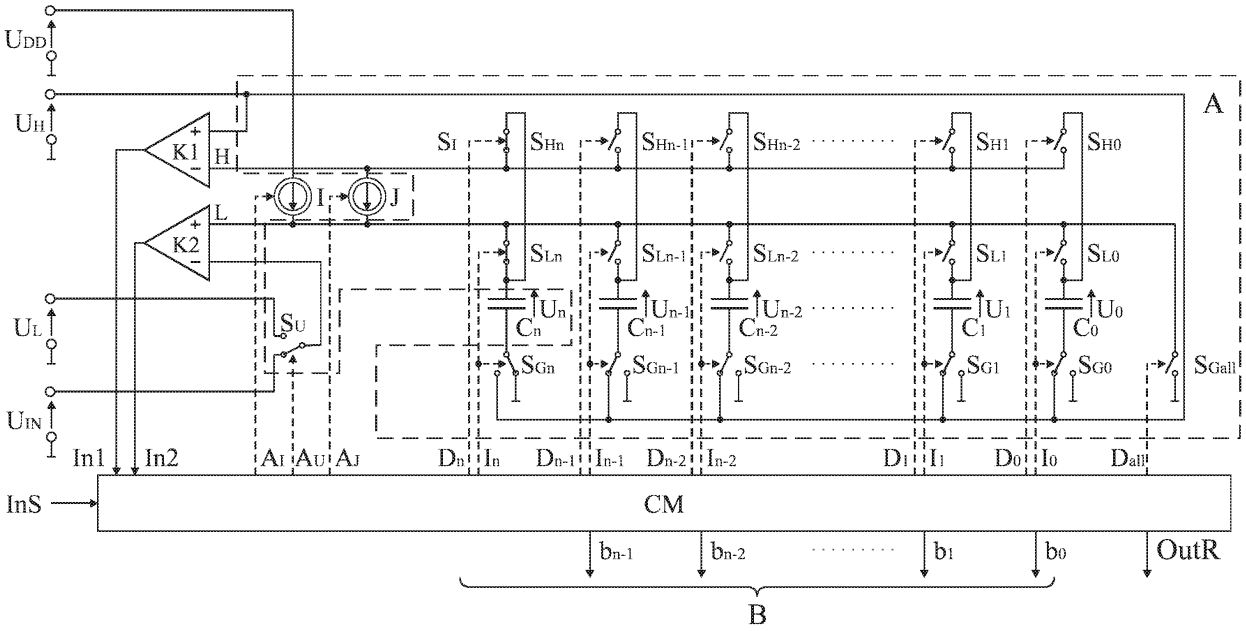
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Fig. 16

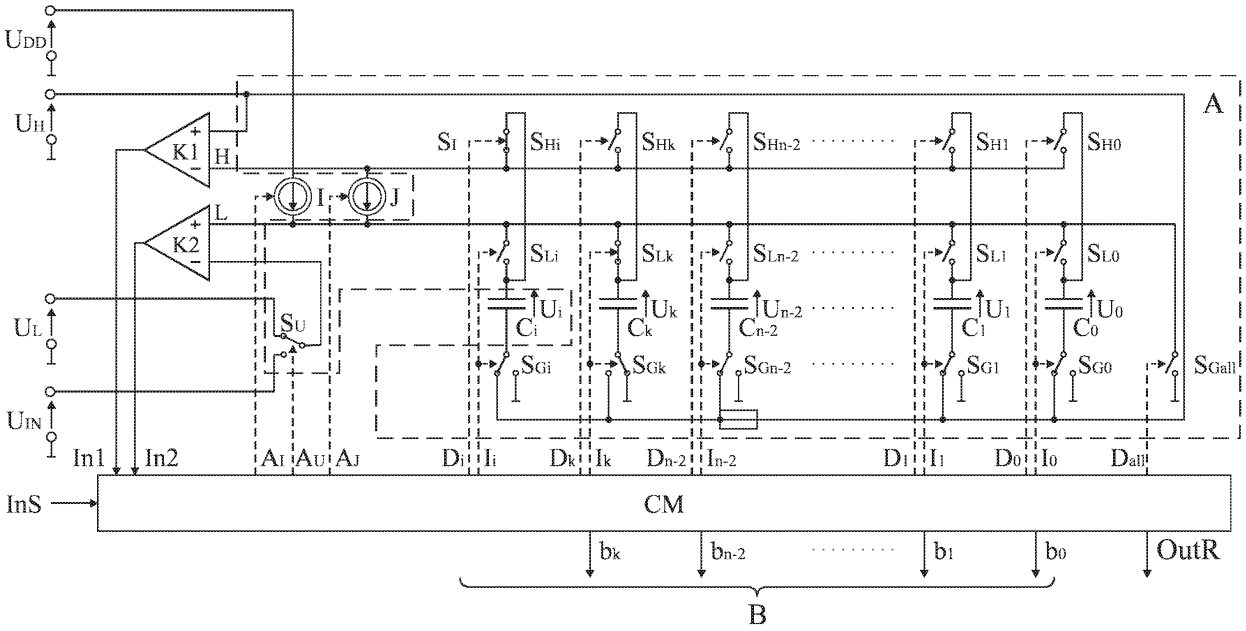
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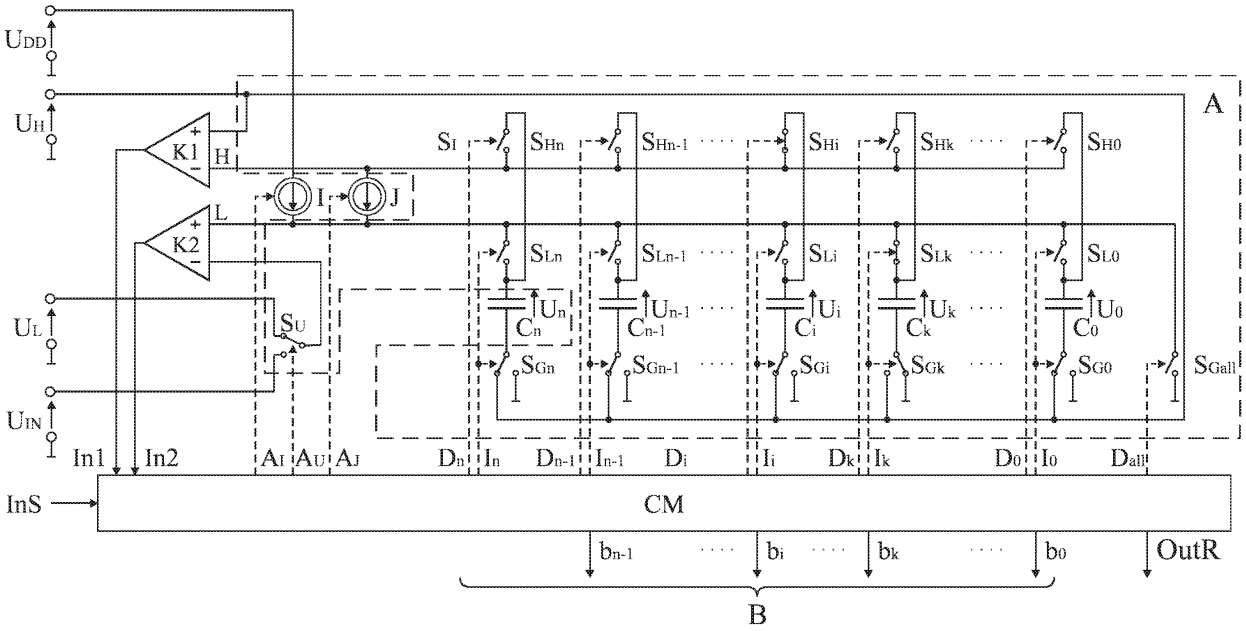
Fig. 17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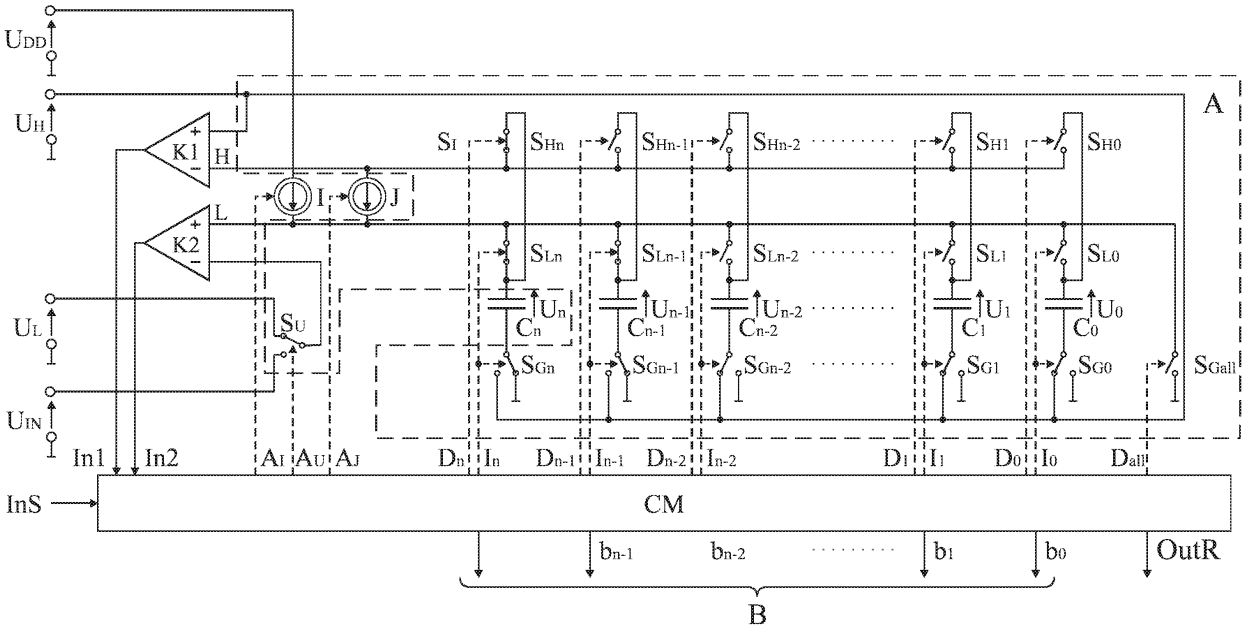
I0
Dall
InS
CM
bn-1
bi
bk
b0
OutR
B

Fig. 18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UL
UIN
K1
K2
H
L
I
J
SU
SI
SHn
SHn-1
SHn-2
SH1
SH0
SLn
SLn-1
SLn-2
SL1
SL0
Un
Un-1
Un-2
U1
U0
Cn
Cn-1
Cn-2
C1
C0
SGn
SGn-1
SGn-2
SG1
SG0
SGall
A
In1
In2
AI
AU
AJ
Dn
In
Dn-1
In-1
Dn-2
In-2
D1
I1
D0
I0
Dall
InS
CM
bn-1
bn-2
b1
b0
OutR
B

Fig. 19

REFERENCES CITED IN THE DESCRIPTION

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